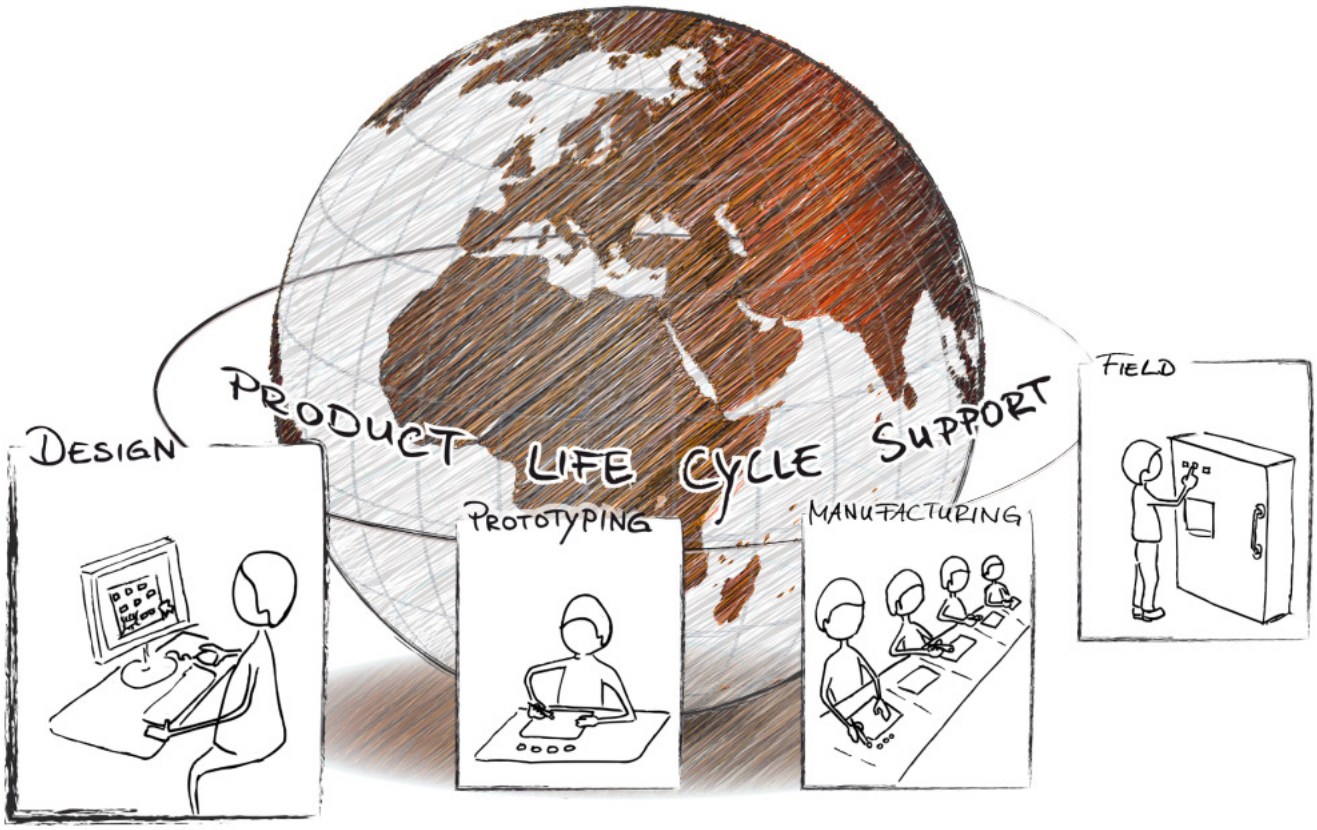
JTAG/Boundary Scan · Design for Testability

Foresighted Board Level Design for Optimal Testability



GOPEL electronic

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Table of Contents

A short Introduction to JTAG / Boundary Scan

1. Why should you care about JTAG / Boundary Scan?

- Here are some of the reasons why:
- Regain test access
  (think of test access problems with BGA, multi-layer PCBs, internal-only signal traces [no vias / test points])
- Reduce cost of test
  (reuse tests throughout the product life cycle, no or simplified fixtures, less expensive equipment, ...)
- Debug prototypes, detect defects and diagnose faults down to pin level; reduce time-to-market
- Precise diagnostics and fast test execution in manufacturing tests, improve yield and productivity
- No / reduced physical stress (probing), less risk for damage of the unit under test
- In-system configuration/programming for CPLD, Flash, serial EEPROM, on-chip memory [MCU, MPU] (just-in-time programming, no inventory management issues and costs related to programmed devices)
- Simplify test strategy and reduce cost by combining test methodologies
- Reduce or eliminate NDF (No Defect Found) issues with in-field, in-system test and error logging, reduce cost of repair / warranty returns;

In summary: lower cost, increased quality.

JTAG / Boundary Scan was the first test methodology to become an IEEE standard. The standard number is IEEE 1149.1 and its initial version was balloted on and approved in 1990. This standard defines features to be designed into an integrated circuit that provides access to its digital I/O pins from the inside of the device. This allows circuit nodes on the PCB to be accessed with device internal test features, rather than with a bed-of-nails fixture or with moving probes. (GOEPEL electronic offers a software tool explaining IEEE 1149.1 features and their functions. It is available free of charge upon request.) With these built-in test features, Boundary Scan helps us to access circuit nodes that may not be accessible when using external physical access methods with probes. This is especially important when considering the wide use of high-density device packages and components with hidden solder joints (such as BGA, micro BGA, and so on). Boundary Scan also has the potential to shorten time-to-market since it can be used very early in the product life cycle, potentially without the need for any bed-of-nails fixture or flying probes.

Furthermore, Boundary Scan can be used throughout the whole product life cycle, since test vectors can be applied with very simple test equipment. Special circuitry to execute Boundary Scan tests can even be embedded on a Printed Circuit Assembly (PCA) for use at the system level, for example as part of power-on self tests for systems out in the field. Boundary Scan tests can be developed very rapidly and early in the design cycle, typically as soon as a schematic design of the UUT is available, even prior to having the layout of the PCB finished.

The primary application, for which Boundary Scan was initially developed, was to detect and diagnose manufacturing defects related to connectivity at the board level, such as stuck-at-0 and stuck-at-1 faults, open solder joints, and shorted circuit nodes. Today, the test access port defined in IEEE 1149.1 is used for many additional applications, such as in-system programming, access to built-in self test, on-chip emulation and debug resources, and system level test.

JTAG stands for Joint Test Action Group, which was a group of interested parties that set out to develop the test methodology that became IEEE 1149.1. Since then, many standard development efforts built on the original work by reusing features defined in 1149.1. One such standard is IEEE 1149.4, which defines device features supporting the test of analog circuits. Another example is IEEE 1149.6, which defines test resources used to verify AC-coupled networks, improving testability of technologies such as differential networks. IEEE 1532 defines in-system programming features accessible via the test access port defined in 1149.1, essentially providing a common method to program devices from different vendors. A number of additional standardization efforts related to JTAG / Boundary Scan have recently been completed (e.g. IEEE 1149.7, IEEE 1500, IEEE 1581) or are under way (e.g. IEEE P1149.8.1, IEEE P1687, IEEE P1838, SJTAG).

This document focuses on design for test guidelines related to Boundary Scan. Contact GOEPEL electronic to request additional background information about Boundary Scan and related technologies.

Boundary Scan – Board Level Design for Testability (DFT)

Introduction

The design rules discussed in this document are guidelines that support optimal test coverage and reliable execution of Boundary Scan tests. Circumstances of a specific printed circuit board (such as signal trace layout, functionality, cost considerations, available “real estate” on the PCB) may necessitate deviations from these guidelines.

A basic understanding of IEEE 1149.1, Standard Test Access Port and Boundary Scan Architecture, often referred to in short as JTAG or Boundary Scan, are beneficial. Of particular interest are the Test Access Port (TAP) signals, the workings of the TAP controller, and Boundary Scan capabilities of I/O pins.

Component Selection

2. **If possible, select IEEE 1149.1 compliant ICs**

   In general, the more Boundary Scan enabled ICs there are on a Unit Under Test (UUT), the better the achievable test coverage thanks to the additional Boundary Scan pins providing access to the surrounding circuitry. Furthermore, the diagnostics can be improved with multiple Boundary Scan pins connected to the same net (circuit node).

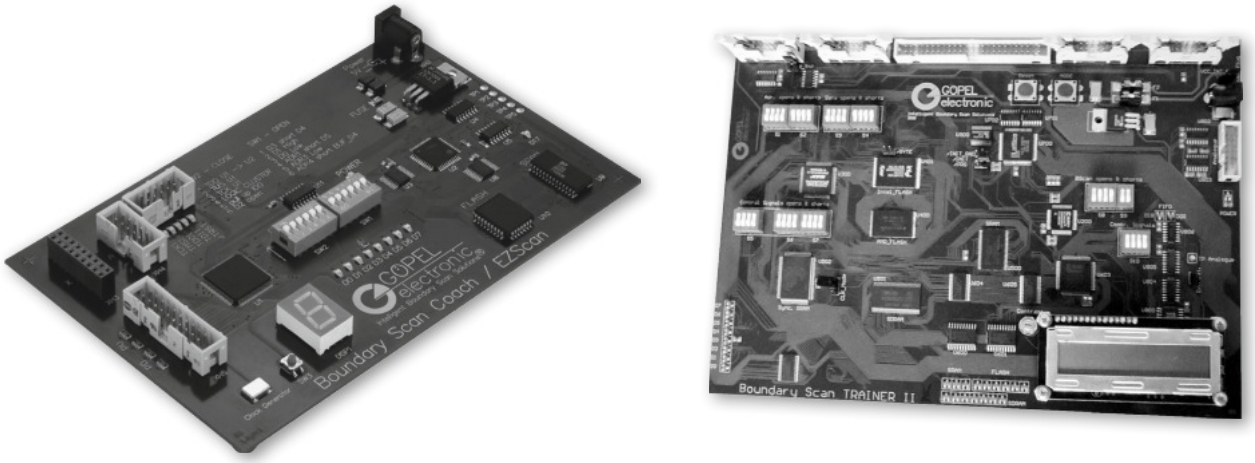


Figure 1: A PCBA (left) with two and another PCBA with seven Boundary Scan devices

   Consider putting logic (combinatorial and sequential) into PLDs/FPGAs, since those type devices typically include Boundary Scan features, while simple logic components don't. If you have influence over the development of ASICs used on your UUTs we strongly recommend you insist on the implementation of Boundary Scan, which will improve test coverage and test development time dramatically.

3. **Request accurate BSDL files from device manufacturers**

   The Boundary Scan test system of your choice should already include a sizable library of Boundary Scan enabled devices. In case of ASICs or new ICs, however, you should request Boundary Scan Description Language (BSDL) files for such devices from the manufacturer early enough to have them on hand when you start the Boundary Scan test development for UUTs involving such devices. Furthermore, inquire that the device vendor has verified the BSDL file.

4. **Verify standard compatibility of the BSDL files**

   Consider use of the BSDL Syntax Checker (www.goepel.com/bsdl-syntax-checker) to verify syntax and semantics of the BSDL file. The same tests are performed when the BSDL file is imported into the SYSTEM CASCON™ device library.

5. **Check BSDL files for compliance conditions and design warnings**

Compliance conditions specify how certain pins need to be controlled in order to enable Boundary Scan tests. This optional section of a BSDL file is identified by the keyword (attribute) COMPLIANCE_PATTERNS.

Design warnings are optional paragraphs of specific requirements for the Boundary Scan ICs, identified by the keyword (attribute) DESIGN_WARNING. An example is the advice of changed Boundary Scan behavior of a configured FPGA.

6. BIST – Built-In Self Tests

Built-In Self Tests (BIST) can help verify the proper function of device internal circuitry or that of external devices and BIST can tremendously improve the fault-coverage achievable with IEEE 1149.1, since Boundary Scan itself in principle does not test the at-speed functional behavior of the UUT. Typically, BIST can be set up and initialized, and the test results (usually go/no-go information) can be read out, through the test access port (TAP) defined in IEEE 1149.1. Information about availability and control of BIST is generally specified as a BSDL extension (although, many device vendors may implement BIST for device level tests but never advertise their existence in BSDL files or datasheets). The optional keyword (attribute) RUNBIST_EXECUTION indicates the existence of BIST in a particular device and describes implementation details of RUNBIST (an optional instruction defined in IEEE 1149.1).

7. IEEE 1532 – Advantages over SVF or JAM/STAPL

IEEE 1532 specifies the in-system configuration features (programming, erase, read, etc.) of compliant PLDs and FPGAs. One key benefit of IEEE 1532 is that it allows the simultaneous handling and concurrent configuration of multiple devices, even devices from different vendors.

Some PLD and FPGA vendors provide BSDL files with and without IEEE 1532 specifications. We suggest you use the files with IEEE 1532 specifications, this way you are free to use these functions if you later choose to do so.

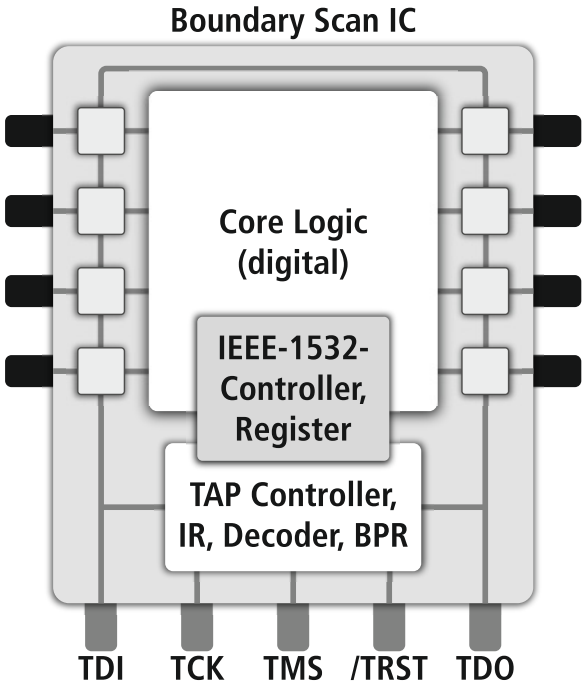


Figure 2: IEEE 1532 device

8. Design for testability is team work

Assemble a team of beneficiaries to discuss the implementation of Boundary Scan at the design stage (beneficiaries include design engineers, production test engineers, field service engineers). Don’t forget to involve management and procurement to evaluate monetary savings throughout the product life cycle.

Layout of the Scan Chain

9. Scan chain (TAP) connector design – be consistent

If you use Boundary Scan to test different types of UUTs, all these UUTs should ideally use the same type of connector and the same pinout for the test access port (scan chain interface) connector. This way the same test bus cable can be used to connect the different UUTs to the test system. Figure 3, below, shows the pinout used by GOEPEL electronic‘s Boundary Scan hardware.

Pin	Signal	Direction	Note
1	TCK	out	
2	GND		
3	TMS	out	
4	GND		
5	TDI	in	must be connected to the UUT‘s TDO
6	GND		
7	TDO	out	must be connected to the UUT‘s TDI
8	GND		
9	/TRST	out	
10			do not use

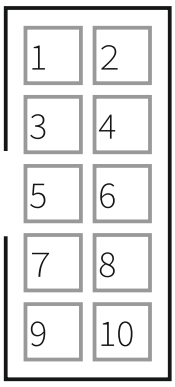


Figure 3: Example Boundary Scan connector pinout

10. Scan chain access

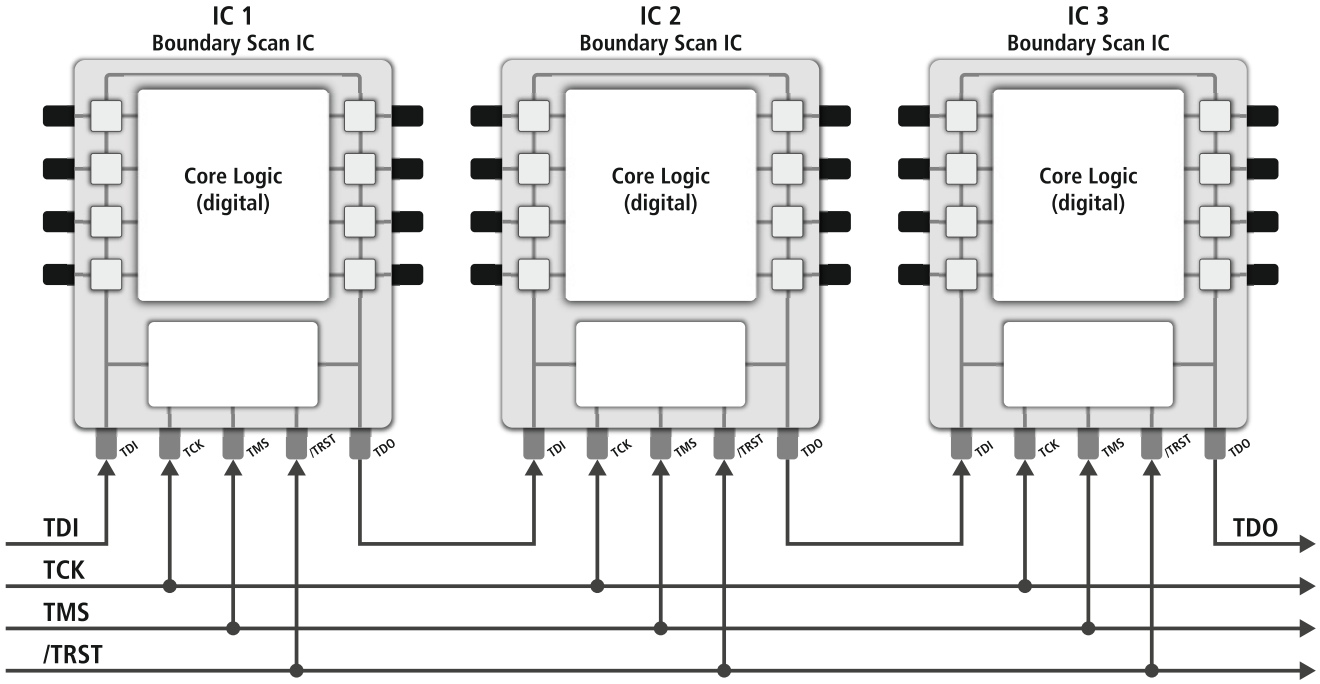
Consider putting the test bus (TAP) connector close to the edge of the PCB (this way a cable plugged into the connector has less impact on the probe movement if Boundary Scan is supposed to be used on a flying probe tester).

In addition to the TAP connector(s), you may also want to route the test bus signals to spare pins on an edge-connector that is also used for functional connections. This would allow access to the scan chain even if the TAP connector is not mounted, or if the TAP connector cannot be reached easily, and it can simplify the test setup (fewer cables to handle, especially when Boundary Scan and functional test are integrated in one test setup).

11. Ensure proper scan chain design

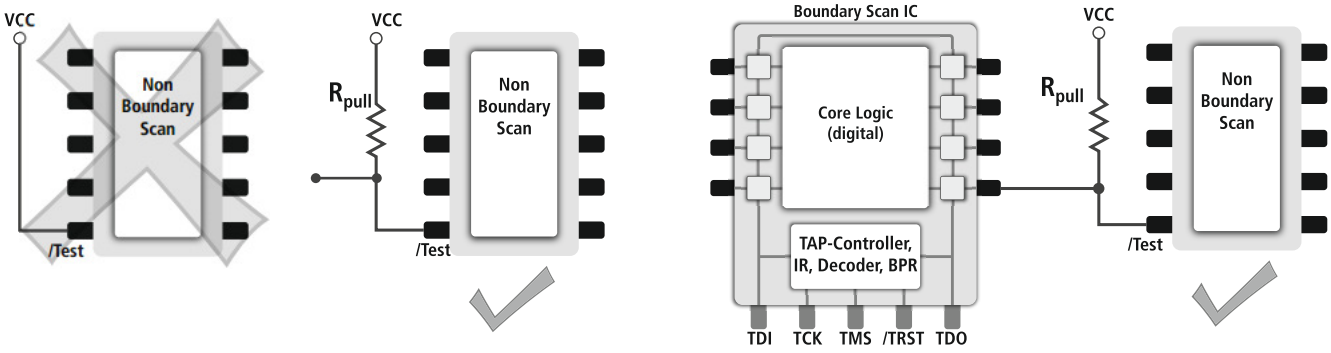
    The most common scan chain design is that of a daisy-chain, where the TAPs of several Boundary Scan devices are connected in series: TCK and TMS on all Boundary Scan ICs are connected in parallel, while TDO of one device is connected to TDI of the next device in the chain. If any of the devices feature a /TRST signal, make sure to bring this signal out to the test bus connector (this is especially important if the /TRST pin will be tied off to GND with a pull-down resistor, because the test system needs to force the /TRST signal to logic high in order for Boundary Scan to work). Never tie off the /TRST signal directly to GND, without a pull-resistor, as this would permanently disable Boundary Scan to work for this particular scan chain.

12. Use pull-resistors to set input pins to default signal levels



    If certain pins (such as compliance enable pins on DSPs or FPGAs, for example) of Boundary Scan ICs need to be kept at a fixed logic level for normal (non-test, functional) mode, make sure to use pull-resistors to do so and provide a test point or connector pin (so that the signal can be forced to the appropriate level for Boundary Scan tests).

    In general, keep in mind that compliance enable conditions specified in BSDL files (or data sheets) need to be satisfied for respective Boundary Scan devices to work. In the BSDL file, look for the attribute COMPLIANCE_PATTERNS (see also DFT guideline 4).



13. FPGA configuration and Boundary Scan

FPGA devices generally don't support Boundary Scan while they are getting configured. This means the configuration of such FPGA devices needs to be inhibited until Boundary Scan testing is completed, or FPGA configuration needs to complete before Boundary Scan tests can be executed. In some cases a configuration of the FPGA is necessary to ensure proper I/O configurations (as required for the communication with other connected devices on the UUT). An un-configured FPGA typically provides bi-directional Boundary Scan cells on every I/O pin, ideal for achieving a high test coverage. When an FPGA gets configured, some of the I/O pin functions may be changed to input only or to output only, or previously single-ended I/O may get grouped to differential I/O - in such cases the Boundary Scan cell assignment and functionality may change, a fact that needs to be considered during the Boundary Scan connectivity test generation. Boundary Scan capabilities that changed based on device configuration need to be communicated to the test system with a post-configuration BSDL file that reflects those changes, since the standard BSDL file supplied by the device vendor specifies Boundary Scan resources available when the FPGA is not configured. Typically, these post-configuration BSDL files can be generated with the same software tools (from the FPGA device vendor) used to create the FPGA design. Consider test specific designs for FPGAs (especially if the functional design reduces the bopundary-scan test coverage) and CPLDs - such designs could provide test functions that cannot be obtained with Boundary Scan alone. E.g. a CPLD or FPGA could be loaded with some board design specific test functions and then - after the standard Boundary Scan connectivity test is executed - the respective CPLD or FPGA could be put into functional mode and these test functions could be executed (perhaps even in conjunction with Boundary Scan in other devices) in order to obtain additional fault coverage (for example for functional cluster tests). Even small CPLDs which provide a test access port (TAP) for in-system configuration but no Boundary Scan test capability (no Boundary Scan cells connected to I/O pins and no EXTEST function) can be reconfigured temporarily for test purposes, for example with a simple pass though network or with some test logic functions such as defined in IEEE 1581. After the Boundary Scan tests are completed, such FPGAs and CPLDs can then be configured with their functional design.

14. Mind the PCB layout of test bus signals

When routing test bus signal traces on the PCB layout, keep in mind that the signals need to be clean, dramatic overshoots need to be avoided and ringing needs to be minimized. TCK, TMS, and /TRST should be laid out similarly (e.g. trace length and width). Avoid a star-type layout and provide proper signal termination to avoid reflections. Avoid crosstalk by keeping signals at an appropriate distance and/or by shielding signals. Follow layout design rules generally applied to high-speed signals.

15. Optimize test bus signal terminations

TCK, TMS, and /TRST need to be treated as high-speed signals which require clean signal edges and little overshoots. The optimum approach is a bus layout, where the termination is provided at the last device. A typical termination scheme is a small serial resistor (e.g. in the range from 20 to 40 Ohm) at the driver (GOEPEL electonics' Boundary Scan controllers include such serial resistors on TAP drivers) and a pull-down resistor (with or without a pull-down capacitor) at the last Boundary Scan device in the chain (the device farthest from the TAP connector on the UUT).

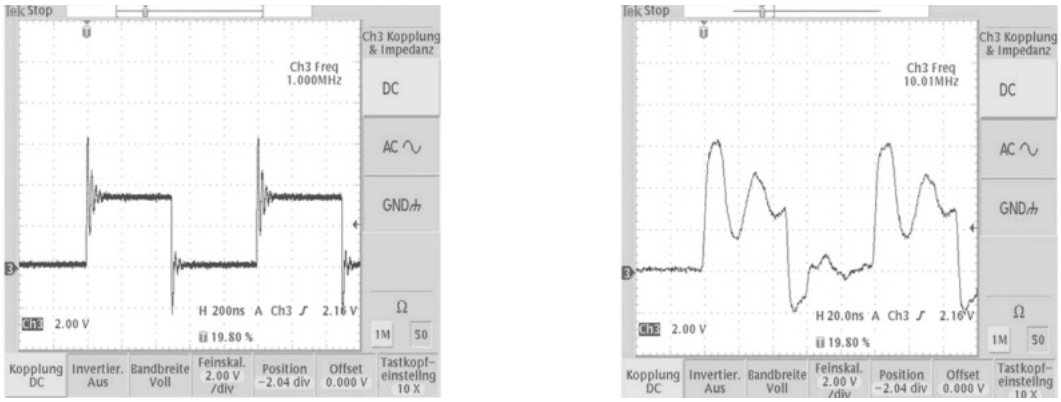


Figure 6: Considerable overshoots due to signal reflections

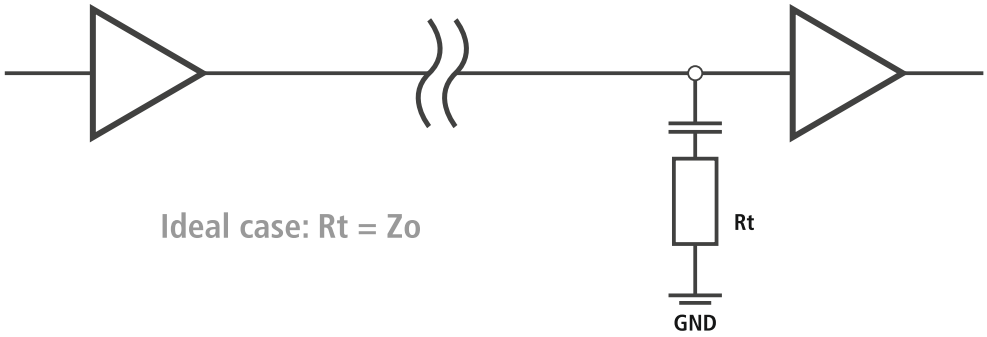


Figure 7: Termination with pull-down resistor and capacitor

The ideal values for Rt and Ct shown in Figure 7 always depend on the actual conditions on the UUT (voltage, signal length and layout, etc.) and should be calculated as accurately as possible. Common values for Rt are 68 Ohm to 100 Ohm (Rt should match the impedance

Zo of the transmission line, considering both the test bus cable and the trace on the UUT) and Ct is often in the range up to 100 pF (when calculating the appropriate value for Ct, the termination resistor Rt, the transmission line impedance Zo, and the driver impedance need to be considered). Such an AC termination (including Rt and Ct) is beneficial only for the TCK signal. The purpose of Ct is the reduction of quiescent power dissipation in Rt.
Even though required by IEEE 1149.1, not all Boundary Scan devices have an internal pull-up resistor at their TDI pin. To avoid or identify test problems later on, consider including a pull-up resistor (e.g. somewhere between 5 kΩ to 10 kΩ) on the signal connecting TDO of one device to TDI of the next device.
The /TRST signal should have a weak pull-down resistor (e.g. 10 kOhm) to ensure that Boundary Scan stays inactive during functional use of the UUT (never tie off the /TRST signal directly to GND, without a pull-resistor, as this would permanently disable Boundary Scan to work for this particular scan chain). The Boundary Scan system needs to access the /TRST signal and drive it high for the duration of Boundary Scan tests.

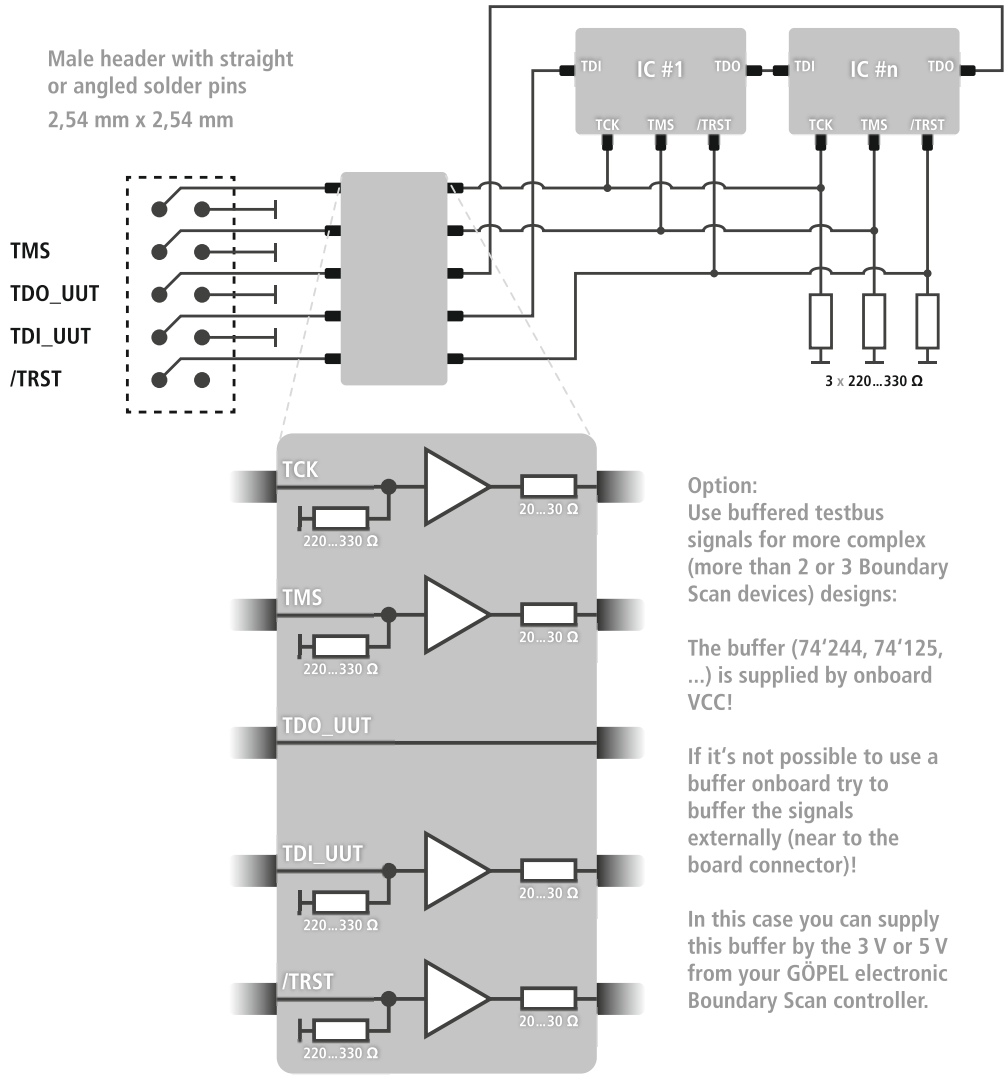


Figure 8: Example design of a complete scan chain including termination

16. Number of Boundary Scan devices and supply voltage levels on the UUT

If a UUT includes multiple devices in a scan chain, the driver strength of the Boundary Scan controller hardware needs to be able to handle this fan-out. For scan chains with just three to five devices it is generally recommended to include a buffer on the UUT to drive the test bus signals. Any such buffer devices must be the non-inverting kind - an inversion or the test bus signal levels would inhibit the proper function of Boundary Scan tests. Mind proper termination techniques. If the Boundary Scan devices on the UUT work with different voltage levels, and lower-voltage ICs cannot handle the higher test bus signal levels other devices use, make use of level shifters to adjust the signal levels accordingly or keep the respective devices in separate scan chains.

The decision of when to shift signal levels or when to buffer the test bus signals depends on conditions on the actual UUT (number of Boundary Scan ICs, I/O technologies, etc.).

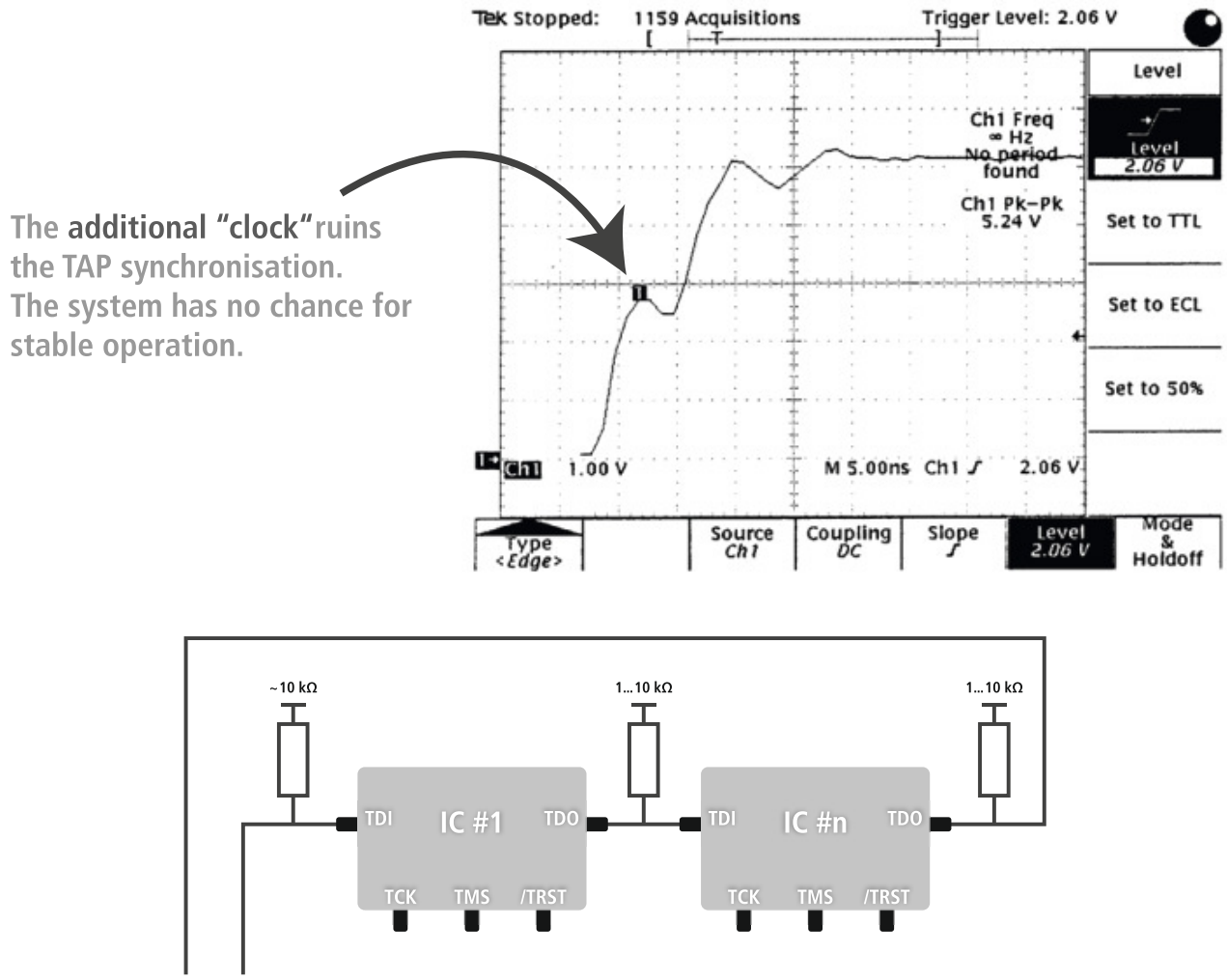
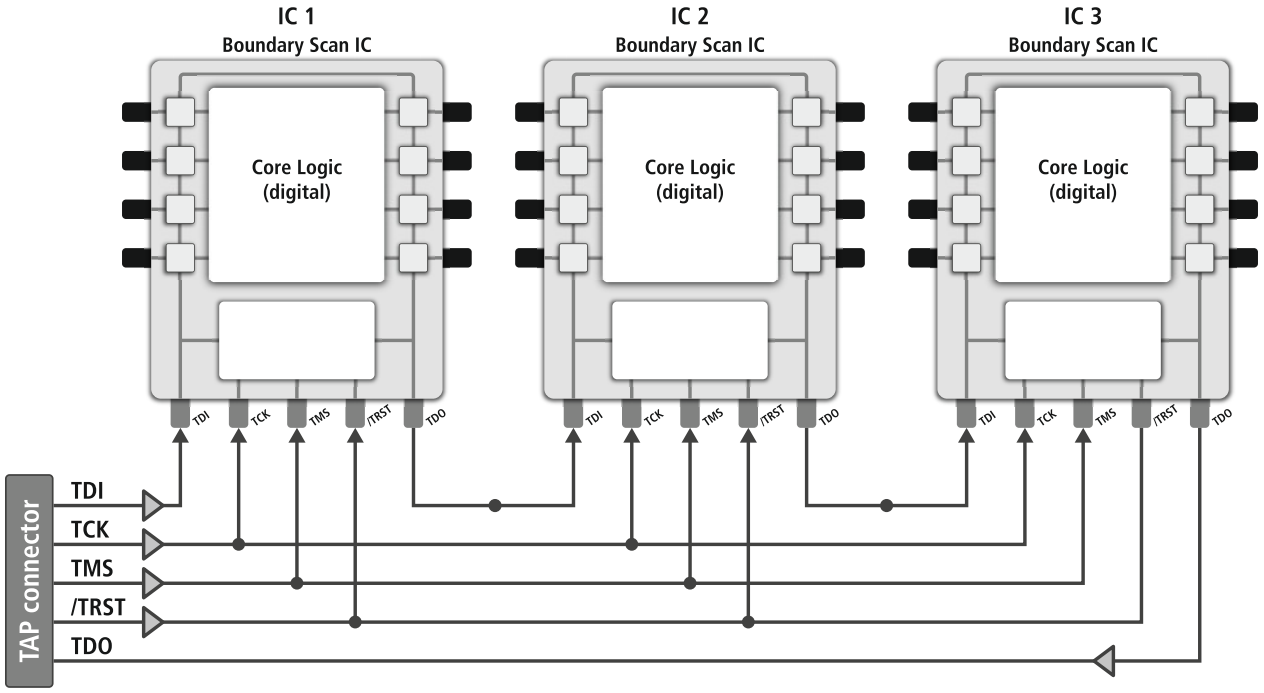


Figure 9: „Extra Clock" at the rising edge due to inappropriate termination

17. Provide means that can help test engineers in quickly locating scan chain errors

Add a test point to each of the signals connecting TDO of one device to TDI of the next device in the scan chain. IEEE 1149.1 provides means to diagnose scan chains. E.g. a simple scan

through the instruction register is sufficient to determine whether or not the TCK, TMS, and TDO signals are connected and working properly (the first bit read at a particular device's TDO would be a logic high, and the second bit a logic low value). For the identification of the actual culprit in a non-working scan chain, a test point in the signal path connecting TDO of one device to TDI of the next device in a daisy chain can be very beneficial.



18. Testing of assemblies of multiple boards

If the UUT is an assembly of multiple boards or modules, and there are UUT variants where some boards or modules may not be mounted, with Boundary Scan devices included on the various modules, it is important that any missing modules do not break the scan chain for the whole assembly. One way to handle this is illustrated in figure 12 below..

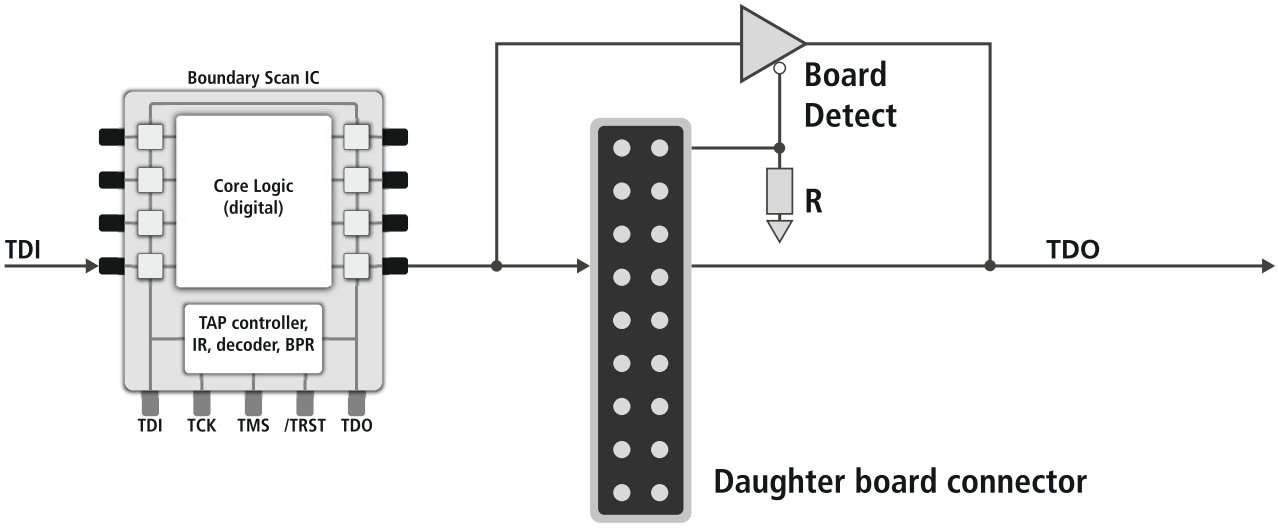
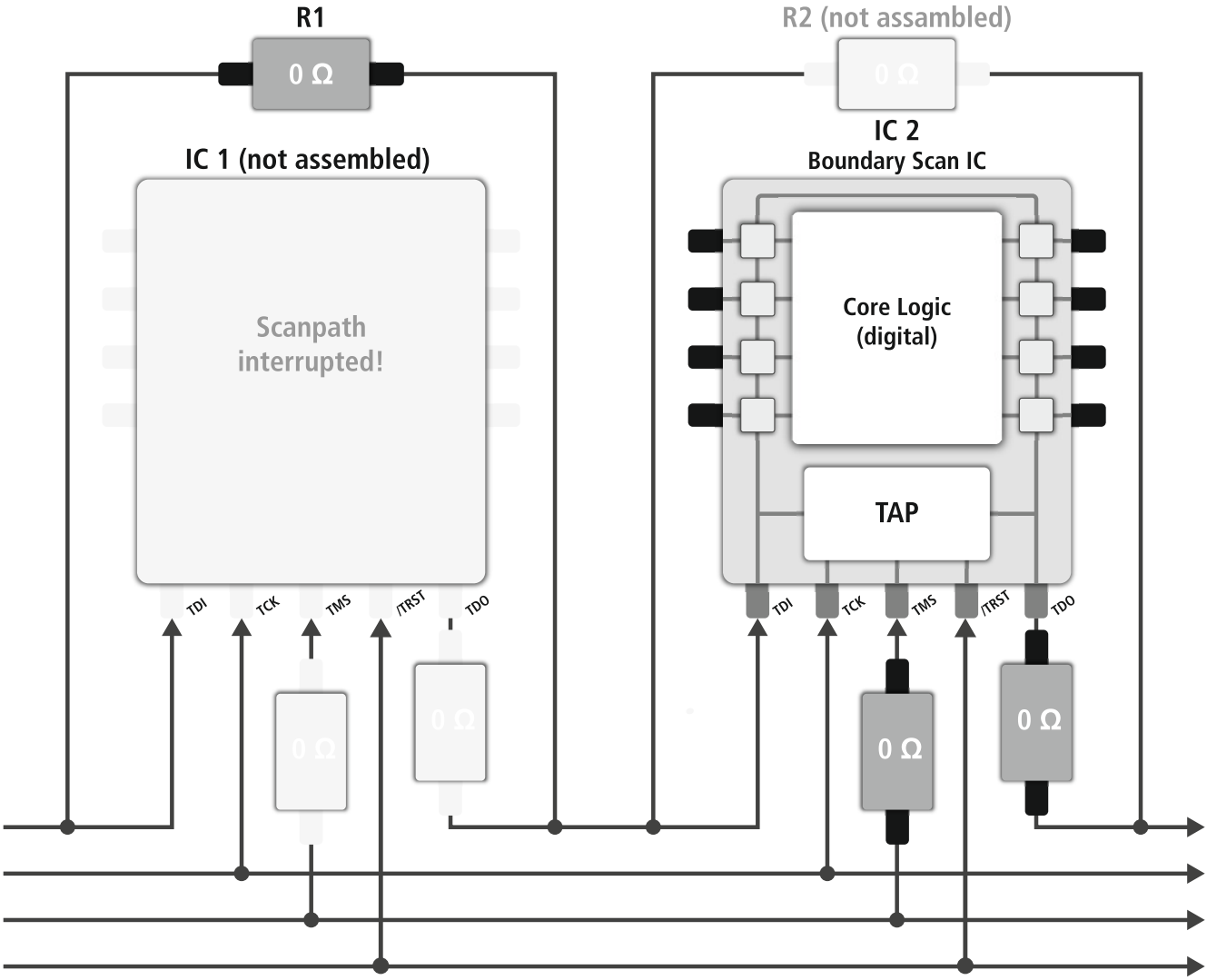


Figure 12: A missing daughter card must not break the UUT's scan chain

19. **Provide means to bypass Boundary Scan devices that are not mounted or are not fully compliant**

    Some UUT variants may call for one or more Boundary Scan devices not to be mounted. In order to keep the scan chain intact in such cases, at least a bypass resistor connecting the respective TDI and TDO signals is needed.



If Boundary Scan ICs not fully compliant to IEEE 1149.1 are included on a UUT, it is best to keep them in separate scan chains, so that they can be excluded or included in tests as appropriate and possible, without impacting other Boundary Scan devices on the UUT.

Non-Boundary Scan Signals and Non-Boundary Scan ICs

20. Provide access to important control signals

Important control signals on a UUT include reset, clock, power control, and watchdog signals.

Keep in mind that reset signals, depending on the design, potentially can inhibit one or more Boundary Scan devices from functioning in test mode, resulting in scan chain errors. Clock signals should be Boundary Scan accessible (and controllable) in order to allow control of synchronous ICs (such as DRAM). Power control signals may enable or disable power supply to the whole or parts of the UUT. If Boundary Scan devices are not powered up, the scan chain won't work and Boundary Scan testing won't be possible. Watchdog devices expect a trigger (e.g. an "alive" signal generated by a controller device on the UUT) in certain time intervals. If such a trigger is not detected by the watchdog device, it typically generates a reset or puts the UUT into a safe state, at which point Boundary Scan testing may be disabled, too. Provide means to disable the watchdog, if possible with Boundary Scan.

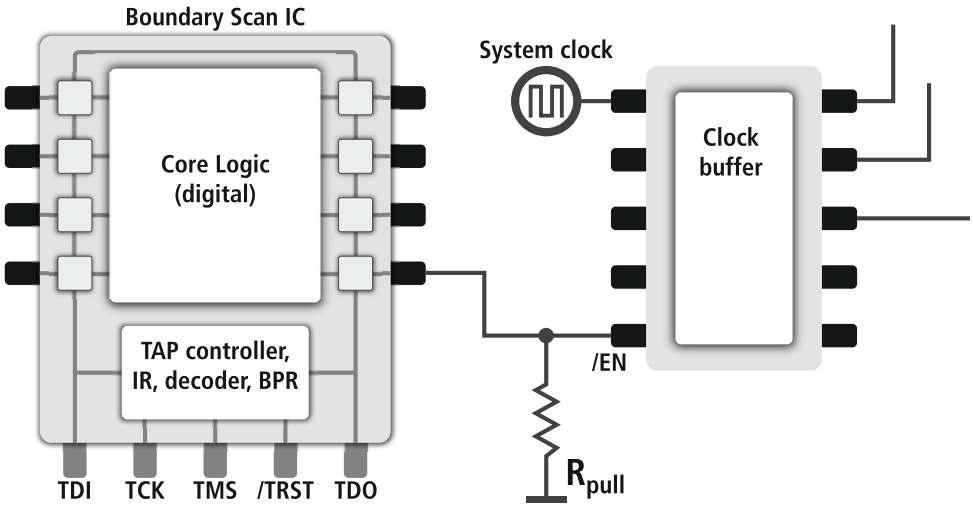


Figure 14: Example for clock control

21. Provide means to disable non-Boundary Scan ICs

In order to test data busses on a UUT with Boundary Scan, it is important to be able to deactivate outputs of non-Boundary Scan devices connected to those data busses. Bus contentions and collisions need to be avoided, i.e. no more than one pin must drive a specific circuit node at any given time.

22. Whenever possible, make logic clusters BScan controllable and observable

In order to test a logic cluster through Boundary Scan, its inputs and outputs need to be connected to Boundary Scan pins of surrounding devices. For good diagnostics, keep clusters as small as possible. In some cases it may be possible and beneficial to put the logic into a programmable logic device (PLD) which itself supports Boundary Scan.

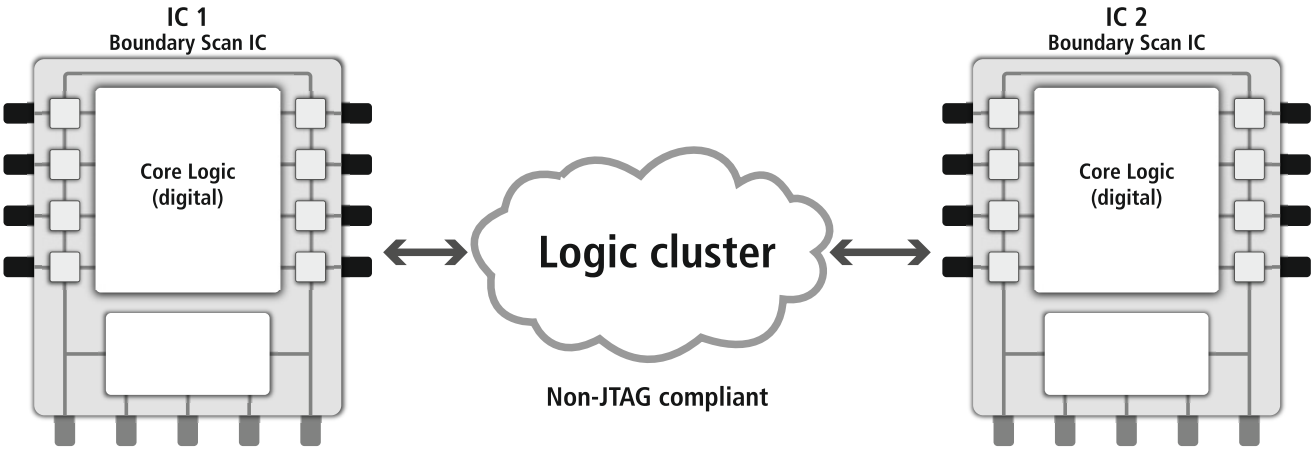


Figure 15: Logic cluster surrounded by Boundary Scan ICs

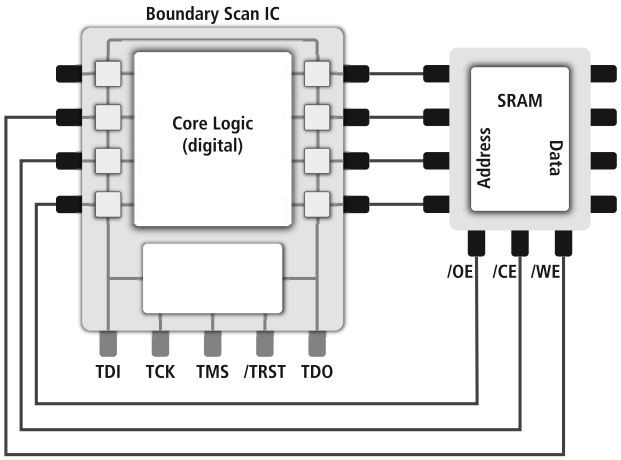
23. Spare Boundary Scan pins

Take advantage of spare Boundary Scan pins (e.g. unused pins on a FPGA or CPLD) by connecting them to otherwise untestable parts of the UUT, such as enable and direction signals on buffers, or control signals on other, non-Boundary Scan devices, or even signals inside logic clusters. Even if this approach does not always improve the test coverage dramatically, it does in most cases enhance diagnostic details.

24. Access to all signals of memory ICs

Ensure that all signals on memory devices are connected to – and can be controlled by – Boundary Scan pins (this includes the clock input on synchronous memory). In general, buffer, latch, or simple logic devices between the Boundary Scan device controlling the memory and the memory device itself can be tolerated and controlled as part of the test sequence, but this may require additional test development effort. Direct Boundary Scan access to the memory device simplifies test development and provides better diagnostics. If possible, use a Boundary Scan enabled (and IEEE 1149.1 compliant) memory device. Alternatively, future memory devices may implement test features defined in the new IEEE 1581 standard.

Figure 16: Memory and Boundary Scan ICs



Programming

25. Access to programmable, non-Boundary Scan devices

Ensure that all control signals on programmable devices (such as serial EEPROM or Flash EEPROM) are accessible from Boundary Scan devices. The programming time for Boundary Scan based in-system programming primarily depends on two parameters: the length of the scan chain and the TCK frequency. Both parameters have an impact on the data throughput between Boundary Scan IC and EEPROM. For the shortest possible programming time with pure Boundary Scan access, the scan chain must be as short as possible and the TCK frequency must be as high as possible.

Avoid address latch configurations if possible, as they typically complicate the access sequence to the EEPROM and may lengthen the programming time significantly.

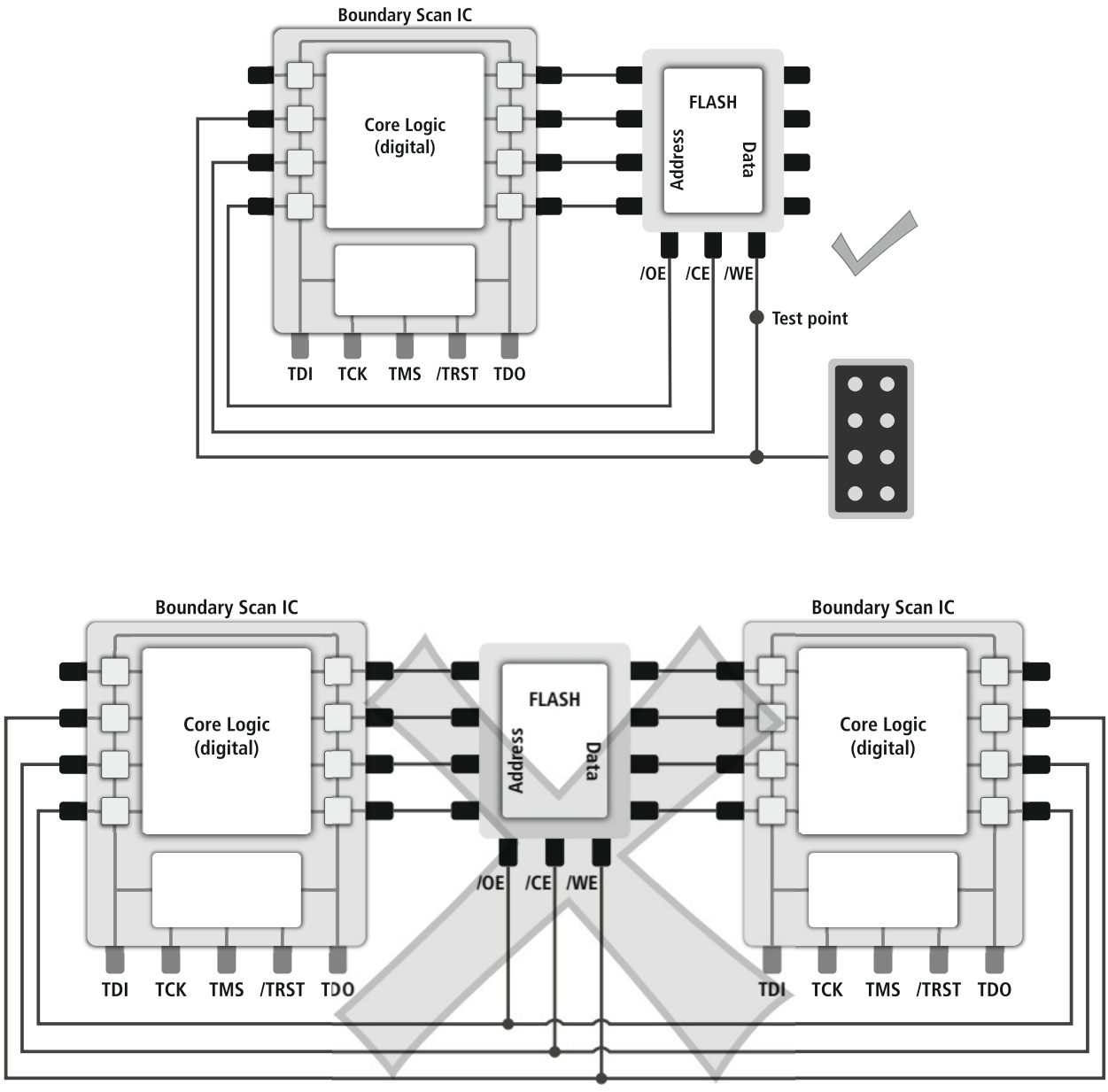


Figure 17: Flash memory access from a single Boundary Scan IC

26. Enhance programming speed with direct access to Write Enable pin

The Flash programming time can be reduced significantly by utilizing direct access of the Flash device's write enable signal (through a test point or an edge connector pin) in order to control this signal with a parallel I/O from the test system (rather than controlling this signal with Boundary Scan access). A precondition for this approach is the ability to disable any Boundary Scan drivers on this circuit node (net) on the UUT.

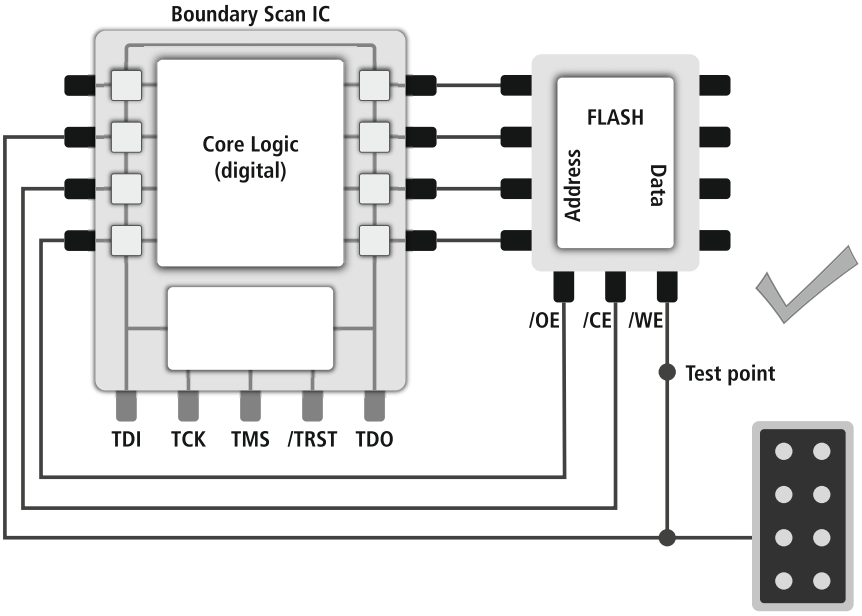


Figure 18: External control of /WE Signals

27. TCK frequency

In order to reduce the programming time, a single Boundary Scan device should have access to all signals on the target memory device. If this Boundary Scan device is in a scan chain with other devices, then the device with the lowest maximum TCK frequency determines how fast the pattern can be shifted through this scan chain. If the maximum TCK frequency supported by the Boundary Scan device used to program the target memory device is much higher than the maximum TCK frequency for other devices in the scan chain, it can be beneficial to create a separate scan chain for the faster Boundary Scan device(s).
Another aspect to be considered is the signal transmission time, in particular the time between a falling edge on the TCK signal on the Boundary Scan controller and the corresponding signal change on TDO as detected by the Boundary Scan controller. Make sure your Boundary Scan hardware can compensate for these signal transmission delays so that they don't limit the maximum TCK frequency that can be applied to a particular UUT, especially if the test bus cable is relatively long (several feet long).

Extending Boundary Scan Test Coverage

28. Utilizing Boundary Scan throughout the product life cycle

For quality management system (QMS) purposes, it is useful to reserve a few bytes of Flash memory for board specific data, such as PCBA type and version, manufacturing date, serial number, rework/repair history, and other important information. The respective Flash device should be accessible via Boundary Scan for in-system programming purposes.
Boundary Scan, in general, is applicable throughout the entire product life cycle. Once various PCBA and modules are assembled, Boundary Scan can provide an access mechanism for system level connectivity test, in-system programming and reconfiguration, power-on self tests, and more. If PCBAs are returned from the field for repair, Boundary Scan can be an important and powerful debug and diagnostic tool.

29. Utilize test modes in non-Boundary Scan ICs (e.g. NAND-Tree)

Some non-Boundary Scan devices offer special test features that often can be beneficial for board-level manufacturing tests and for diagnostics. Don't inhibit the use of such test modes by permanently disabling them. Boundary Scan access to complex non-Boundary Scan devices can be used to provide at least some basic test capabilities, such as reading a device ID or some register values. If such non-Boundary Scan devices include a test mode, such as a NAND- Tree or NOR-Tree, this device can actually be included in Boundary Scan controlled connectivity tests, allowing the detection and diagnosis of open pins and shorted signals (e.g. due to solder bridges) that otherwise may not be easily diagnosed.

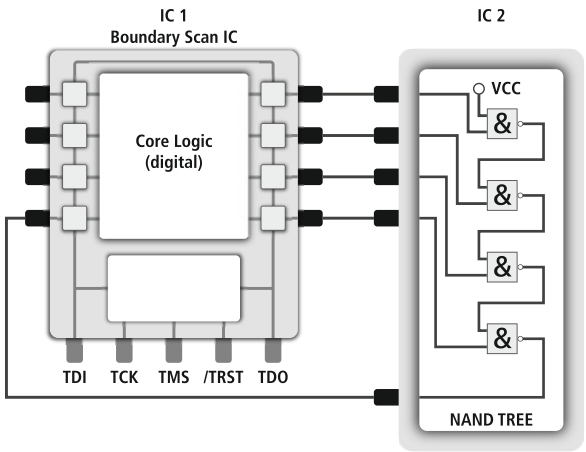


Figure 19: NAND-Tree test

30. Test of analog circuitry

Connect the digital sides of analog/digital converters (ADC) and digital/analog converters (DAC) with Boundary Scan devices. This way analog circuitry can be involved indirectly in Boundary Scan tests. Some ADC/DAC devices even have integrated IEEE 1149.1 Boundary Scan capabilities. IEEE 1149.4 defines test resources for analog and mixed-signal Boundary

Scan. While IEEE 1149.4 compliant off-the-shelf components are very hard to find, it may be a good idea to include these test capabilities in your own mixed-signal ASICs.

Figure 20: DAC test

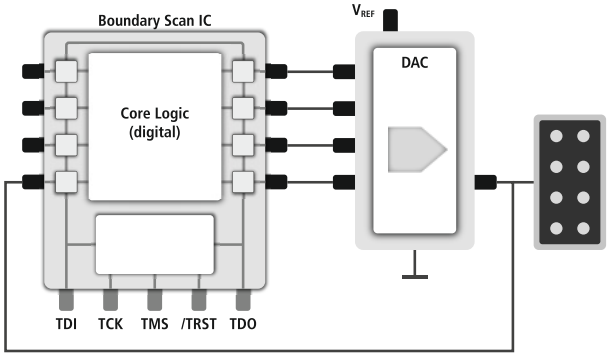
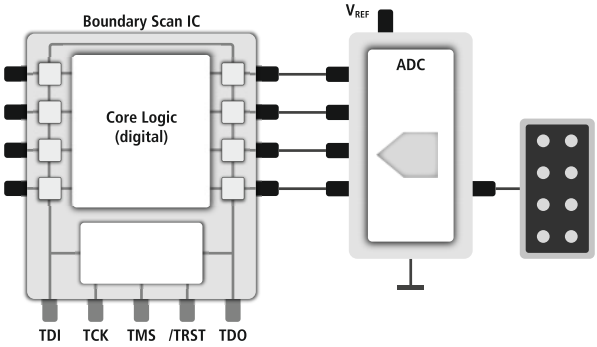


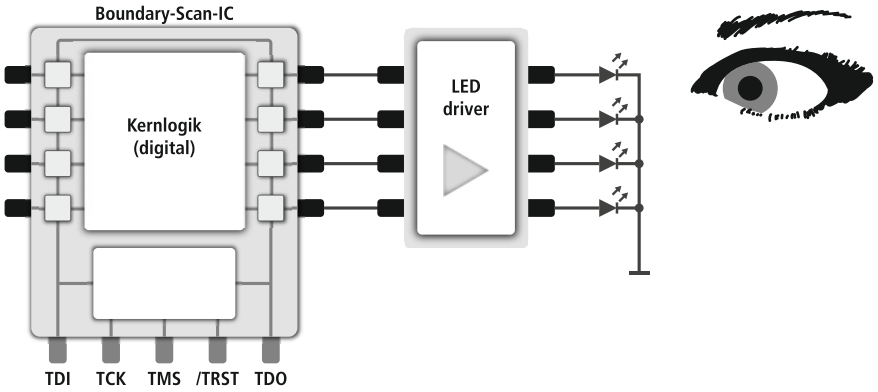
Figure 21: ADC test



31. Test of optical components

Optical components, such as LEDs or LCD displays, for example, can be included in Boundary Scan tests by having an operator or even a camera observe their proper function. Precondition is that such devices are directly or indirectly controlled by Boundary Scan enabled devices.

Figure 22: LED test



32. Test of switches

Switches (including push buttons, flip switches, relays, etc.) can be tested as part of Boundary Scan tests as well. Such cluster tests are either written manually or generated based on device test models. For example, a Boundary Scan IC can read the pin connected to the switch signal a number of times, expecting a signal change within a certain time limit (the switch, of course, needs to be actuated by an operator or some other means).

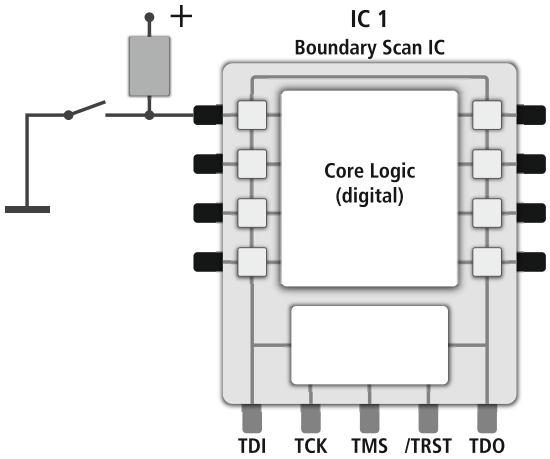


Figure 23: Switch test

33. Test of clock signals

Clock signals can be tested with Boundary Scan in regards to whether or not the clock is active. Boundary Scan can detect if a clock signal is toggling, but it cannot measure the actual clock frequency. A Boundary Scan IC reads the pin connected to the clock signal a number of times, expecting a number of signal changes (e.g. detecting a minimum of X logic high and X logic low states out of Y signal captures) within a certain number of attempts. If the clock signal does not change state, a respective error message can be provided.

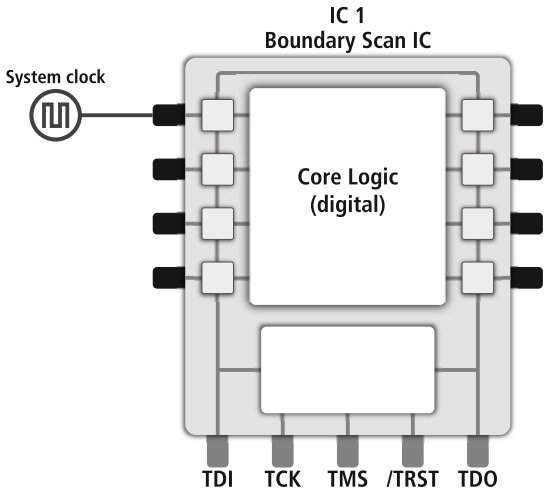


Figure 24: Clock signals

34. Improving the test coverage with I/O tests

The UUTs test coverage can be extended by connecting peripheral connectors to tester I/O channels, or by using loop-backs, including them in the connectivity test. While loop-backs are an inexpensive and simple solution, the best test coverage and diagnostic support can be obtained with I/O modules.

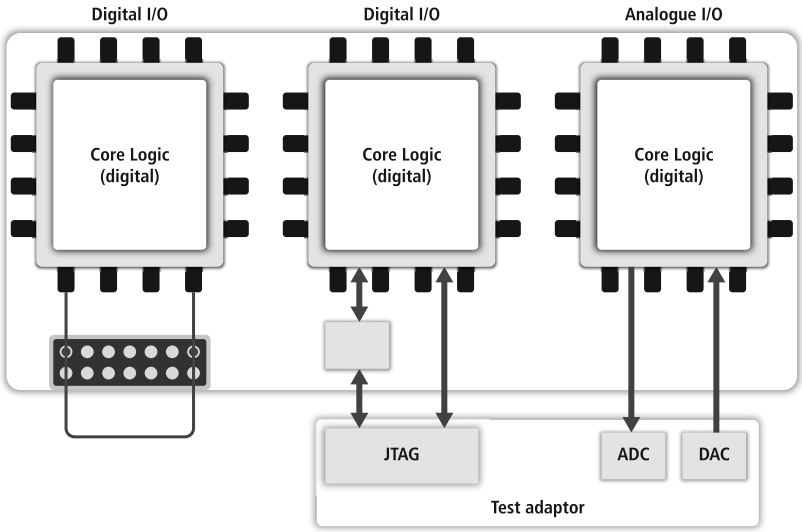


Figure 25: Including peripheral connectors in connectivity tests

35. Improving test coverage with at-speed tests (VarioTAP® and VarioCore®)

Boundary Scan is a quasi-static test methodology. which means it may not be able to detect some dynamic defects. Mixed-signal circuitry and widely used high-speed serial interfaces, for example, cannot be tested with basic Boundary Scan tests. Such circuit parts can be

covered with advanced test technologies such as VarioCore® (IP for PLD/FPGA) and VarioTAP® (interlaced Boundary Scan and emulation test).

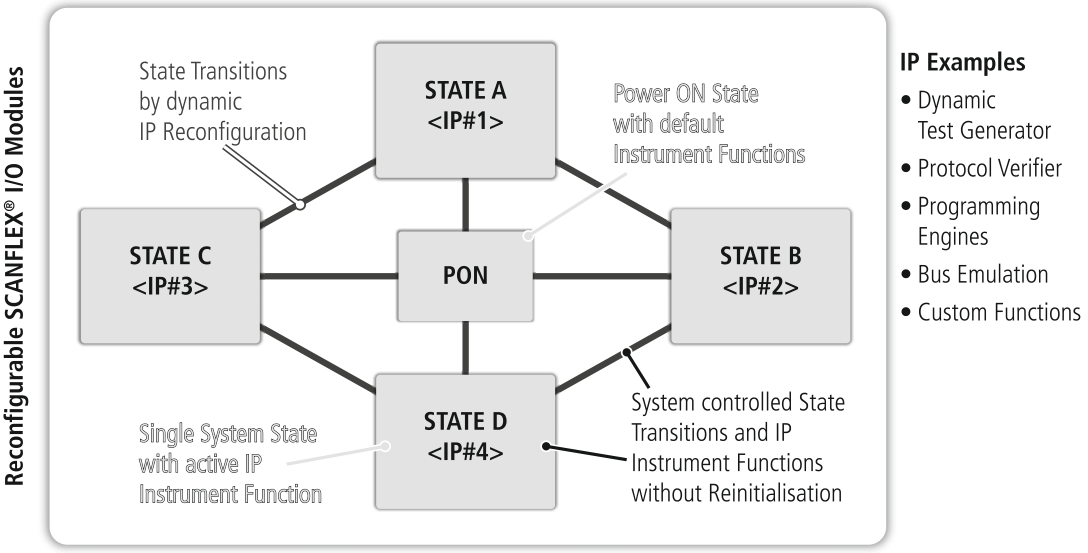


Figure 26: Reconfigurable VarioCore® I/O Module

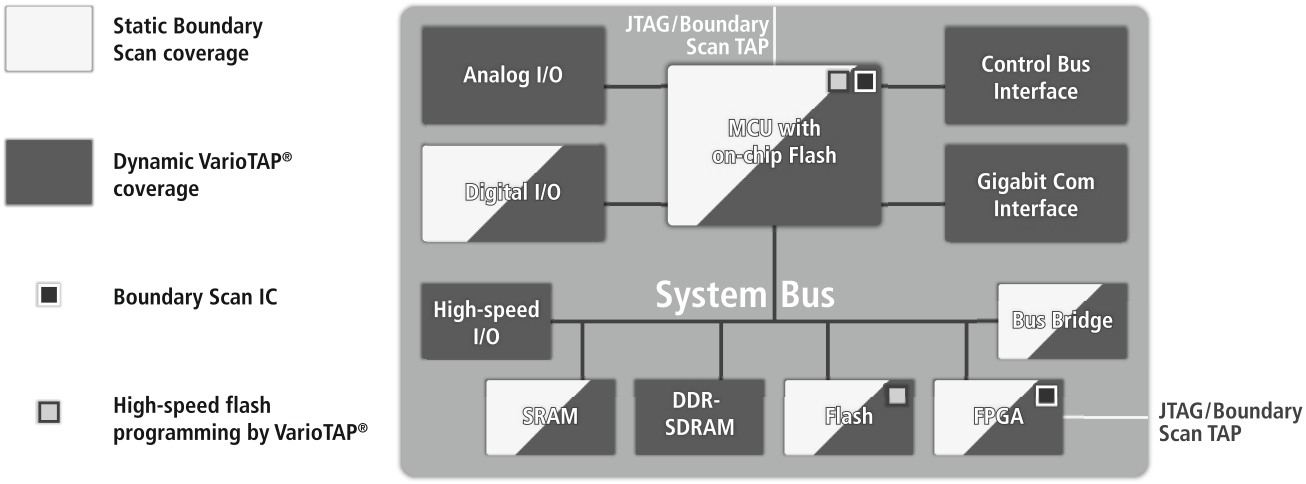


Figure 27: VarioTAP® on-chip programming, on-board programming, emulation test, and interface test

36. Improving test coverage by combining various test methodologies

Depending on the technology and complexity of the UUT and the test philosophy in place, Boundary Scan can be combined with other test methodologies. Such combinations can eliminate disadvantages of the individual test methodologies.

In case of in-circuit testers, Boundary Scan can reduce the number of nodes that need to be accessed with nail probes, simplifying the bed-of-nail fixture and reducing its cost.

For flying prober testers the test time can be reduced by eliminating test steps for parts of the UUT that can be tested with Boundary Scan (such as tests for opens and shorts on digital circuit parts).

Automated optical inspection can be used to check for presence, orientation, and alignment of components prior to electrical tests, which can enhance the accuracy of diagnostics. Furthermore, combining AOI and Boundary Scan allows the automated and more thorough verification of optical components (such as LEDs and LCD displays).
Functional testers can benefit from the diagnostics provided by Boundary Scan, simplifying fault isolation and trouble-shooting at the functional test stage.
Use a Boundary Scan test coverage report to determine where test points for physical probe access are not needed. Try to put all test points (test pads) on one side of the PCB (typically the bottom side).
Especially when combining Boundary Scan and flying probe testing, put the test bus connector and power supply connections on the opposite side of the test points, if possible (this way the test bus cable and power cable can be kept outside of the probe area, allowing the flying probes to move more freely than they could if they had to avoid the test bus cable or power cable for the UUT).

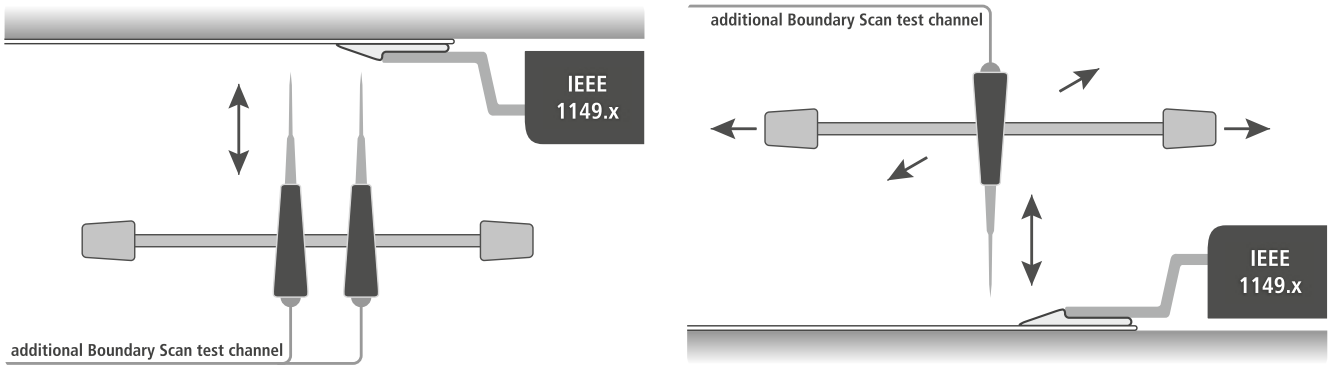


Figure 28: Combination of Boundary Scan and in-circuit test (ICT) or flying-probe test (FPT)

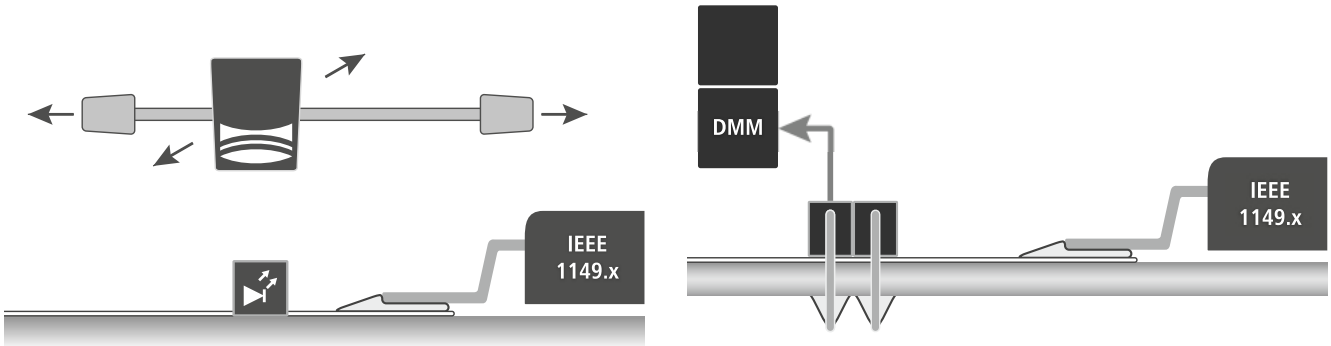


Figure 29: Combination of Boundary Scan and automated optical inspection (AOI) or functional test (FT)

37. System test – Scan Router devices

Boundary Scan is applicable throughout the product life cycle. The test access provided by Boundary Scan can be very beneficial for system level test applications, where a PCBA

is part of a larger assembly (e.g. multiple boards/modules plugged into a backplane). In such applications, the scan chain infrastructure needs to allow the test of individual system modules as well as the test between system modules. Furthermore, any missing modules must not inhibit the Boundary Scan test of other modules in the system. These requirements can be satisfied with so-called scan-router devices, available from various device vendors, including Firecron, Lattice Semiconductors, Telefunken Semiconductors, and Texas Instruments. Such scan router ICs are addressable and link a primary scan chain to one or more secondary scan chains

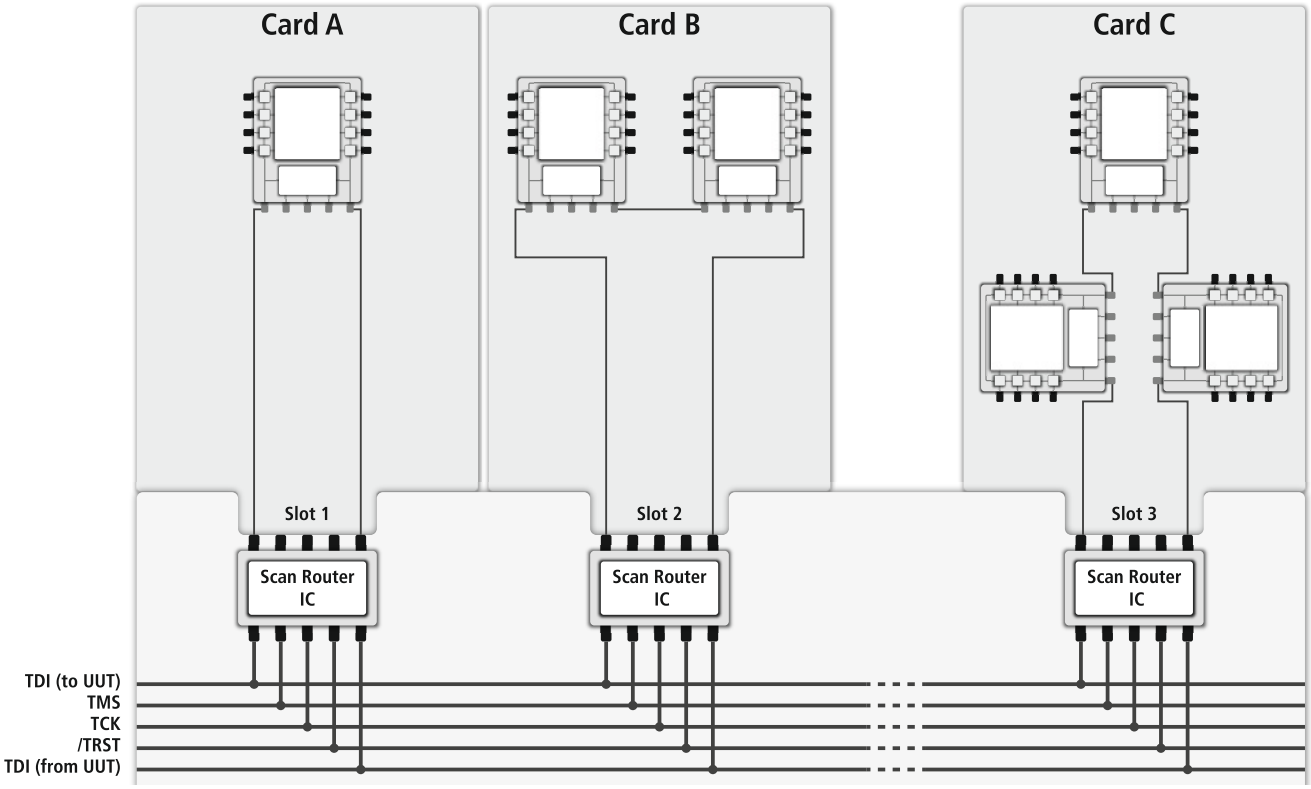


Figure 30: Utilization of Scan Router devices

Selecting a Boundary Scan System

38. Software

Boundary Scan software needs to understand and take into consideration the whole UUT, including non-Boundary Scan circuitry. By analyzing the non-Boundary Scan circuitry and how it interacts with the Boundary Scan devices, ATPG tools can generate safe test pattern. Also make sure the software provides sufficient flexibility and allows adjustments to the test pattern generation, in particular to avoid “Ground-Bounce” effects.

In some cases it can be helpful to edit the generated test vectors or to debug test programs. The Boundary Scan software should offer means to execute test programs in a step-mode. Test programs written in a high-level programming or scripting language provide the necessary flexibility to work around non-compliant device behavior and to handle Boundary Scan test applications beyond the basic connectivity tests. The user should be able to get access to and full control over all Boundary Scan resources (registers, cells, pins, nets, etc.).

Boundary Scan software should allow integrations in third-party test equipment (such as in-circuit testers or flying probe testers) in order to support extended Boundary Scan applications. Such integrations can be realized at different levels, the most advanced of which provides the Boundary Scan software access to tester resources of the third-party equipment to extend the Boundary Scan test coverage.

Ensure that the Boundary Scan software can be extended to support future IEEE 1149.1 related standards. In addition to IEEE 1149.4, IEEE 1149.6, and IEEE 1500, there are new recently released IEEE standards, such as IEEE 1149.7, and standards that are currently in the works, such as IEEE P1687, IEEE P1149.8.1, and IEEE P1838, which are based on Boundary Scan technology and will play an important role in future test applications.

39. Hardware

If the Boundary Scan controller provides multiple TAPs, make sure those TAPs are truly independent and do not get chained together inside the controller. Furthermore, check for programmability of TAP voltage parameters, terminations, and TCK clock speed.

Make sure the Boundary Scan hardware provides dynamic, parallel I/Os for additional test access. Special hardware modules for extending the test coverage (e. g. I/O modules), for integration into other test equipment, or for debug and trouble-shooting assistance, for example, can be very important upgrades to a basic Boundary Scan test system. Some Boundary Scan hardware can be upgraded without any physical hardware exchanges – beneficial if one wants to start with a basic set of hardware functions and add performance and capabilities at some later time, without loosing the initial investment

40. Licensing

    Flexible, granular licensing schemes enable the customization of system configurations. Consider network licensing which allows software to be shared between multiple users and departments, potentially even worldwide. Such “floating licenses” can offer a better utilization of a test system than node-locked licenses.

Glossary

ADC	Analog to Digital Converter
ASIC	Application Specific Integrated Circuit
ATPG	Automatic Test Program Generation
Boundary Scan	Test methodology defined in IEEE 1149.1
BIST	Built-In Self Test
BSDL	Boundary Scan Description Language
CAD	Computer-Aided Design
CPLD	Complex Programmable Logic Device
DAC	Digital to Analog Converter
DfT	Design for Testability / Design for Test
DUT	Device Under Test
EEPROM	Electrically Erasable and Programmable Read-Only Memory
Flash	Type of EEPROM – name derived from method used to erase the memory
FP	Flying Prober
FPGA	Field Programmable Gate Array
FT	Functional Test
ICT	In-Circuit Test
IEEE 1149.1	IEEE Standard Test Access Port and Boundary Scan Architecture; IEEE standard for digital Boundary Scan test
IEEE 1149.4	IEEE Standard for a Mixed-Signal Test Bus; IEEE standard for analog Boundary Scan test
IEEE 1149.6	IEEE Standard for Boundary Scan Testing of Advanced Digital Networks; IEEE standard for Boundary Scan test of differential and AC coupled signals
IEEE 1149.7	IEEE Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary Scan Architecture; also referred to as cJTAG or Compact JTAG
IEEE P1149.8.1	IEEE Draft Standard for Boundary Scan-Based Stimulus of Interconnections to Passive and/or Active Components; also referred to as Selective-Toggle or A-Toggle
IEEE 1500	IEEE Standard Testability Method for Embedded Core-based Integrated Circuits
IEEE 1581	IEEE Standard for Static Component Interconnection Test Protocol and Architecture; standard for test features in non-Boundary Scan devices, such as memories
IEEE P1687	IEEE Draft Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device; also referred to as iJTAG or Internal JTAG

IP	Intellectual Property
JTAG	Joint Test Action Group – group of individual and corporate initiators of IEEE Std 1149.1
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
PLD	Programmable Logic Devices
QMS	Quality Management System
RAM	Random Access Memory
SYSTEM CASCON™	Computer Aided SCan based Observation and Node control – integrated software environment for the development and execution of Boundary Scan tests
TAP	Test Access Port
TCK	Test ClocK
TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode Select
/TRST	Test ReSeT
UUT	Unit Under Test

JTAG/Boundary Scan

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