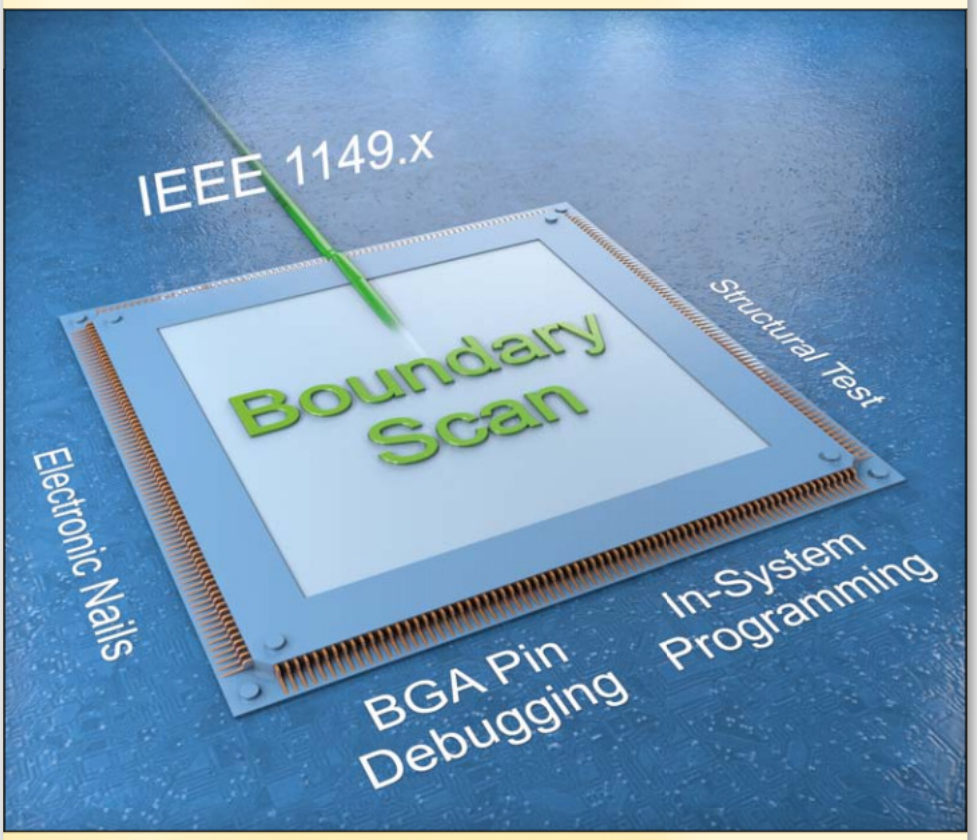
Boundary Scan

Basics and Applications



- **Technology for signal access without nails and probes**
- **Automated test generation and pin-failure diagnosis**
- **Debug of BGA pins and embedded nets**
- **In-system programming of Flash and PLDs**
- **Tool suite completely integrated in SYSTEM CASCON™**

Boundary Scan (IEEE Std. 1149.x) is a revolutionary technology substituting the physical access via nails and probes by means of special on-chip electronics (electronic nails) in conjunction with a dedicated four-wire bus. The method was developed as successor of the digital In-Circuit Test (ICT). It implements the tester's pin electronics directly in the IC design. Boundary Scan provides a multitude of opportunities for structural or functional tests and hardware debug as well as in-system programming. Utilizing the integrated software platform SYSTEM CASCON™, users can implement the full potential of all strategies comprehensively and very flexibly throughout entire product life cycle.

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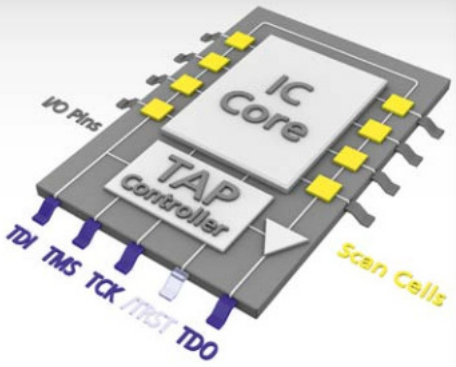
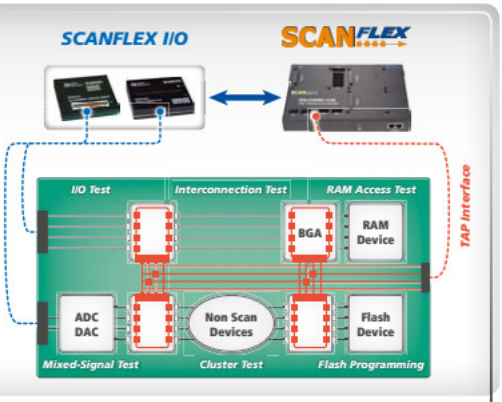
Boundary Scan



TAP: Test Access Port / **TMS**: Test Mode Select / **TCK**: Test Clock / **TDI**: Test Data In / **TDO**: Test Data Out

Boundary Scan IC architecture



Example of a Boundary Scan application with SCANFLEX

Complete Boundary Scan test system with hardware and software

Embedded System Access (ESA) via Boundary Scan

The increasing difficulties in testing modern boards result from the ongoing reduced test access paired with high-speed signal utilization. Modern technologies for Embedded System Access (ESA) provide completely new solutions. Boundary Scan / IEEE 1149.1 has been the forerunner for the standardized test without physical access. The method uses so called Boundary Scan cells, which are chained as register serially shifting vectors in and out via a Test Access Port (TAP). At the board level it is possible to cascade several Boundary Scan components that are controlled by an external controller. In addition to IEEE 1149.1, today there is a number of sub-standards, such as IEEE 1149.4, IEEE 1149.6 and IEEE 1149.7.

Applications for Test, Programming and Debug

The Boundary Scan cells' direct access to the respective pins allows for the defined generation of test vectors and call-up of response vectors. This basic operating mechanism enables numerous procedures, e.g.:

- Interconnection test between Boundary Scan pins
- Access test of RAM pins (sRAM, dRAM)
- Test of differential high-speed signals (IEEE 1149.6)
- Cluster test of non-Boundary Scan components
- Test of peripheral I/O (analogue/digital)
- Test of actuators, sensors and optoelectronics
- Hardware debug / troubleshooting
- Flash programming (NAND/NOR, SPI,I2C etc.)
- Programming of PLDs via SVF/JAM/STAPL

For PLD programming, the four-wire bus is only used as a transfer medium for the programming vectors. All procedures can be implemented very simply and economically compared to conventional techniques such as In-Circuit Test or Flying Prober.

Hardware and Software Support

GOEPEL electronic supports all applications, with over 450 products providing currently the most comprehensive and powerful portfolio on the market. It contains:

- Scalable software platform SYSTEM CASCON
- Scalable hardware platform SCANFLEX®
- Cost-efficient controllers and I/O modules
- Solutions for volume productions

Particular emphasis is placed upon open integration and interaction opportunities with other test strategies and systems for highest fault coverage. Additional information can be found at **goepel.com**.

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GOEPEL electronic GmbH
Goeschwitzer Straße 58/60
07745 Jena/Germany
Tel: +49(0)-3641-6896-0
Fax: +49(0)-3641-6896-944
Email: sales@goepel.com
Internet: www.goepel.com

sales@goepel.co.uk sales@goepelusa.com sales@goepel.asia sales@goepel.fr sales@goepel.in