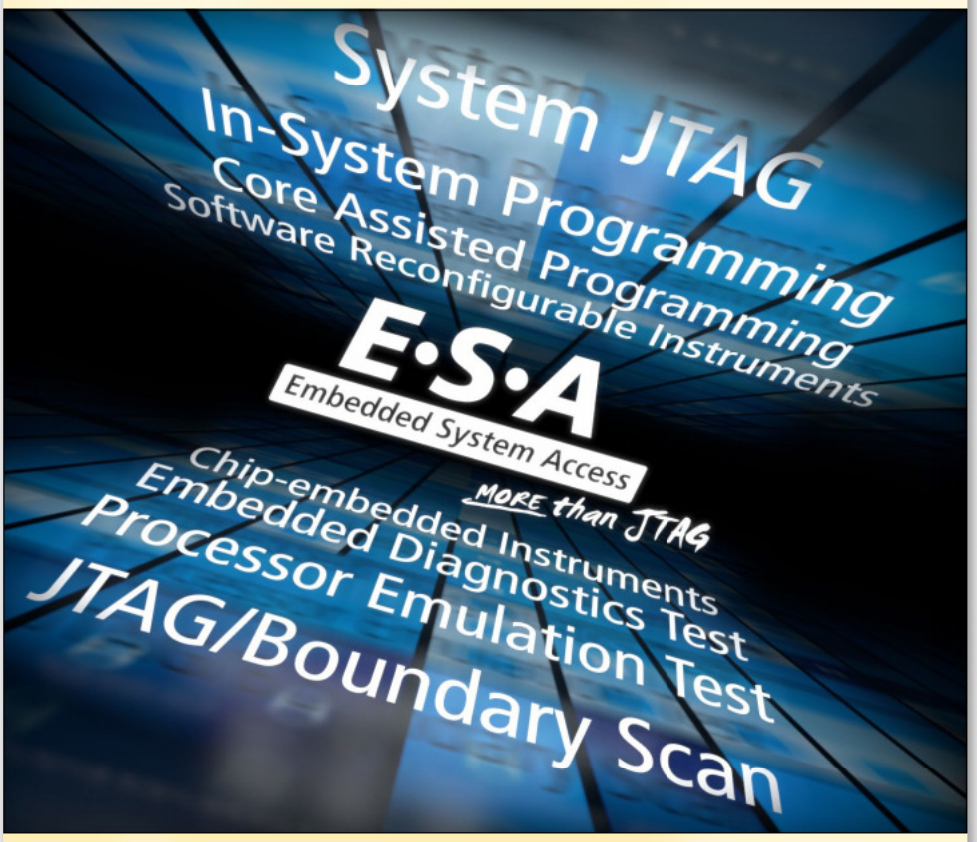
Embedded System Access

A Technology Leader



GOEPEL electronic

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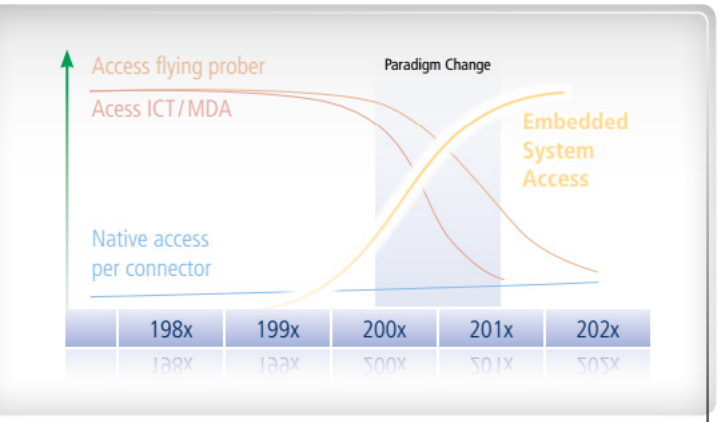
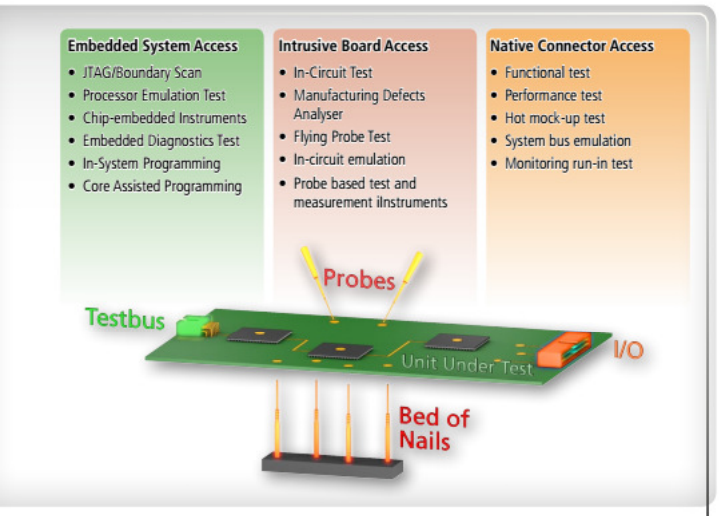
JTAG/Boundary Scan
New Dimensions of Test Access

The Transition towards Multi-Dimensional Access

The problem of testing is as old as the invention of the transistor itself. **Initially**, access was provided only through the native **connectors** on the unit under test (UUT). **Later**, intrusive board access (IBA) in the shape of In-Circuit Tests (ICT) and the Flying Probe Test (FPT) predominated. Nonetheless, these strategies based on **nail contacting can no longer be used for modern modular components** with ball grid array (BGA) and chip scale package (CSP).



Change from the intrusive age to the age of Embedded System Access



Classification of electric access strategies

The key to success: design-integrated system access

In 1990, **JTAG/Boundary Scan** was the first standard to **replace mechanical access, with electrical access** integrated directly into the circuitry. From a current perspective, this standard also paved the way for **Embedded System Access** (ESA). Since then, numerous other ESA technologies and IEEE standards have become available, underlining the **massive paradigm change** that has taken place towards an age of Embedded System Access. In this context, the following ESA technologies are especially noteworthy as far as testing is concerned:

- JTAG/Boundary Scan Test (**BST**)
- Processor Emulation Test (**PET**)
- Chip-embedded Instruments (**IJTAG**)
- Embedded Diagnostics Test (**EDT**)

The common feature of these technologies is that they all use a serial test bus for communication purposes; however, their properties and methods differ entirely.

Property	BST	PET	IJTAG	EDT
Test type	structural	functional	open*	functional
Test speed	static	dynamic	open*	real time
Access through	Boundary Scan IC	processor	IJTAG IC	processor
Fault coverage	static	dynamic	open*	dynamic
Level of diagnosis	pin	net/pin	open*	IC/net
Relatet IEEE standard	1149.x	1149.7 / ISTO 5001	P1687	-

*depending on implementation

In addition, other **ESA technologies** are available especially for **software validation** and for **programming** flash memories, PLDs (programmable logical devices) and micro controllers (MCUs) such as:

- In-System Programming (**ISP**)
- Core-Assisted Programming (**CAP**)
- In-Application Programming (**IAP**)
- FPGA-Assisted Programming (**FAP**)

Advances in integration technologies, right through to 3D integrated circuits, make it possible today to create full systems on one chip in the form of an **SoC** (System-on-Chip). For this purpose, too, **ESA** technologies are **indispensable**. This has made it possible to adopt entirely new approaches to **holistic testing**. These approaches include:

- hierarchical testing (chip, board, unit)
- product life cycle test (laboratory, production, field)
- system level testing (System JTAG, **SJTAG**)

All these principles are based on reusing available test procedures during progressive hierarchical integration as well as in all product life cycle phases. SJTAG also offers a special ESA technology for the integration of the test controller into the system under test.

However, efficient use depends decisively on the performance of the used platforms as well as on the basic product technologies. This includes in particular the ability to openly combine ESA technologies with traditional procedures on a multi-dimensional platform.

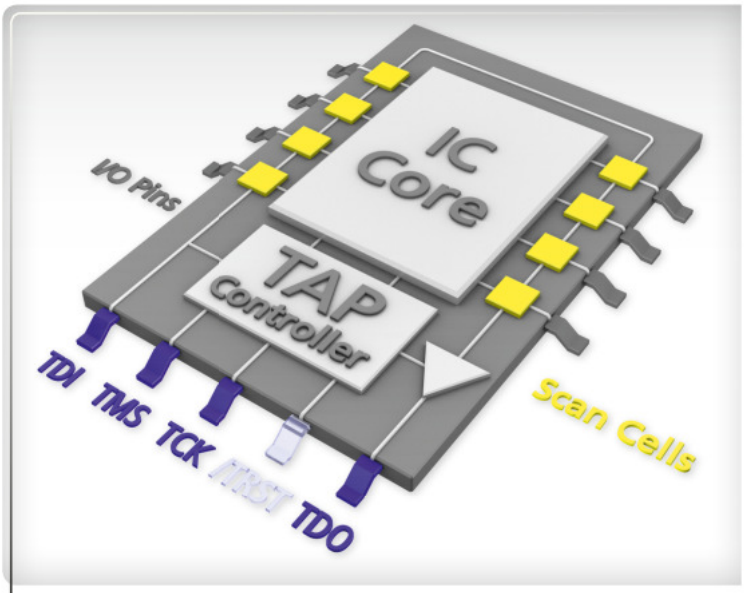
Further information on **Embedded System Access** as well as on technologies and products is available at

goepel.com/**en/esa**

Test-Focused ESA Technologies

JTAG/Boundary Scan Test (BST)

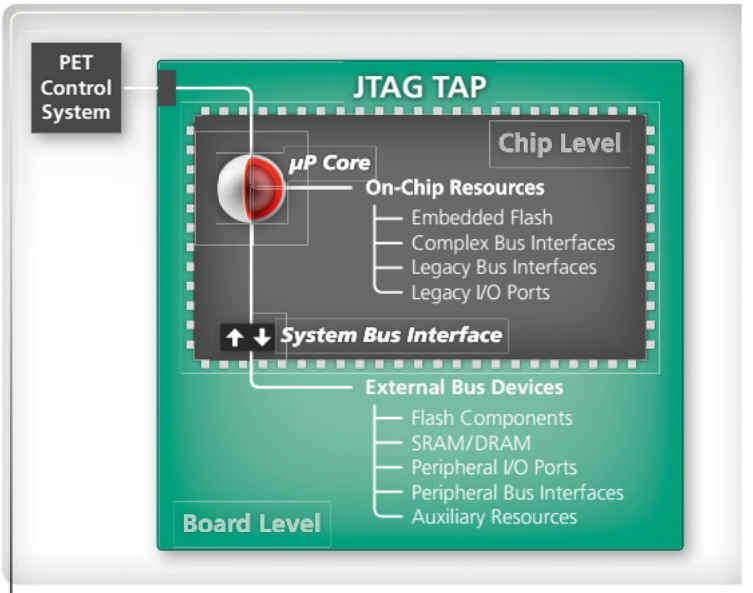
In 1990, **Boundary Scan** was adopted as the IEEE 1149.1 standard. This technology utilises so called boundary scan cells, combined into a Boundary Scan register, as primary access points for a target system's circuit nodes. The Boundary Scan register is accessed and controlled through the Test Access Port (TAP). All vectors are serially scanned. The test bus is comprised of four mandatory signals and a fifth optional reset signal. Boundary Scan is a structural methodology and provides excellent fault diagnostics, especially for connectivity tests on BGA devices, for example. However, since Boundary Scan tests are static in nature, dynamic defects usually cannot be detected, let alone be diagnosed. In addition to IEEE Std. 1149.1, various related IEEE 1149.x standards have been created or are in development to expand fault coverage.



Architecture of a **Boundary Scan device**

Processor Emulation Test (PET)

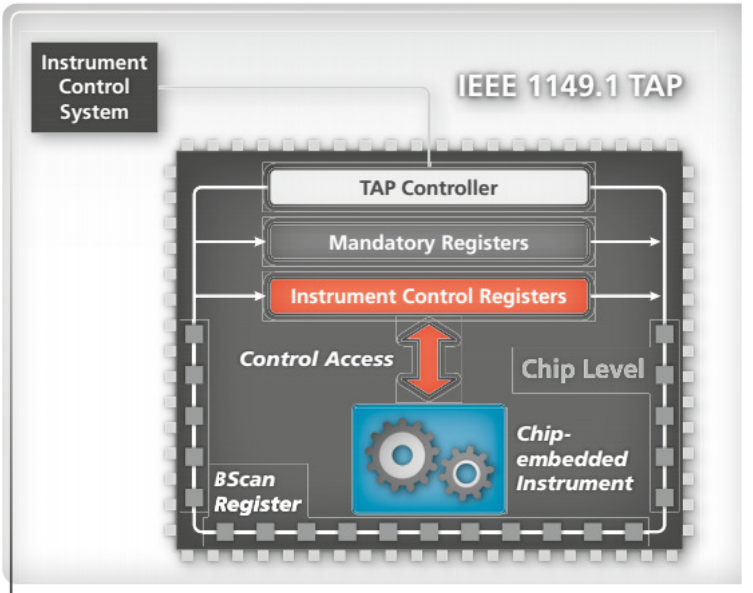
The **Processor Emulation Test** (PET) utilises the debug interface (implemented in many micro processors for software validation) to transform the processor core temporarily into a native test controller. In this case, the processor itself becomes the access point for the connected circuitry in the target system. Remote-controlled through the JTAG interface or some other debug interface, the processor core utilises write and read access to the system bus with respective test vectors in order to manipulate and test the connected internal and external resources and components. No operating system or flash firmware is necessary to accomplish this. The technology can detect both static and dynamic defects; however, diagnostics are limited due to the functional test approach. PET complements Boundary Scan very well and enables or improves especially the test of dynamic components such as DDR-SDRAM, gigabit interfaces, and other non-scannable components at chip, board, and system level.



JTAG control of the native **micro processor as the test center**

Chip-embedded Instruments (IJTAG)

Chip-embedded Instruments are essentially test and measurement intellectual property (IP) blocks integrated into ICs, often accessible through the JTAG port. The functionality of Chip-embedded Instruments is completely open and ranges from simple sensors, to complex signal processing and data collection, through to complete analysis instruments and programming engines. The IP is either integrated permanently in the chip (hard macro) or it can be temporarily instantiated and configured (soft macro) in field programmable gate arrays (FPGA). This specific form is also referred to as „**FPGA Assisted Test** (FAT)" or „**FPGA Assisted Programming** (FAP)." Chip-embedded Instruments have been utilised for years in chip testing, for instance, in the form of a built-in self-test (BIST) IP. Another example is the logic scopes integrated into FPGA for design validation. However, access to these instruments has, until recently, not been standardised, a situation that will change with the launch of the new IEEE P1687 (also known as IJTAG). Hence, standardised Chip-embedded Instruments present an alternative, especially in the field of gigabit analysis, to the traditional testing and measurement instruments with their increasing access problems.

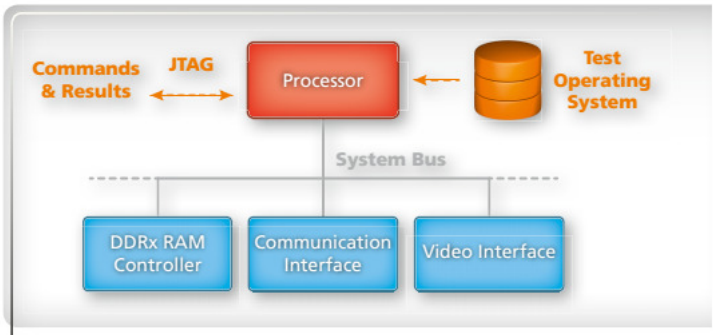


Principle of the **Chip-embedded Instruments**

Details of Further Testing and Programming Procedures

Embedded Diagnostics Test (EDT)

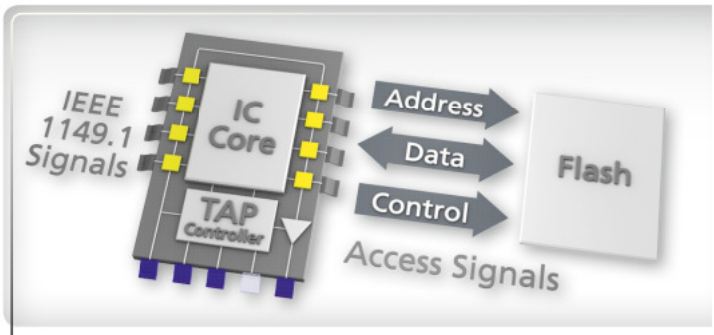
The **Embedded Diagnostics Test** uses the native processor not only to execute tests but also to process diagnostics routines. Since all operations are performed in real time, it is not only possible to detect dynamic faults, but also to optimise performance. For this purpose, special testing software is introduced via JTAG. The software can also be loaded via a fast communication interface. Hence, the native micro processor is the access point to the system. The system's integrated test functions are activated by means of corresponding commands. In the event of a fault, the diagnosis is performed directly in the system. In addition, the EDT can also be used in the form of a resident power-on self-test (POST). Furthermore, the combination of EDT with system JTAG (SJTAG) offers interesting technical options to identify hardcore faults in complex systems.



Principle of the **Embedded Diagnostics Test**

In-System Programming (ISP)

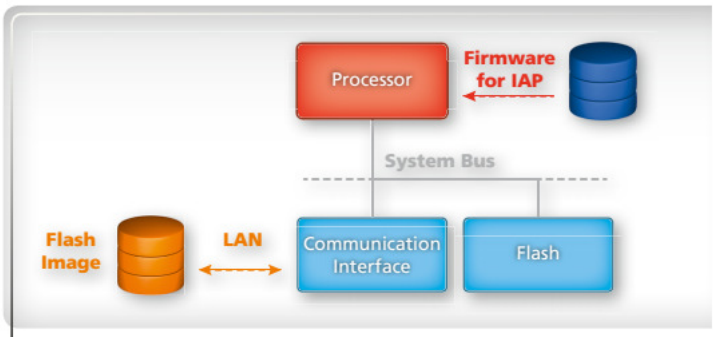
In-System-Programming (ISP) is a collective term for the **programming** of flash devices **by means of Boundary Scan** and for the programming of PLD/FPGA devices through their Test Access port (TAP) and built-in programming registers, while the devices are mounted on the printed circuit board. For In-System Programming of PLD/FGPA, special standards exist, such as IEEE 1532, JESD-71, and an industrial standard called Serial Vector Format (SVF). A new feature in the field of ISP is flash programming through FPGA-based instruments (FPGA Assisted Programming). These are special Chip-embedded Instruments (soft macros), which lead to drastic improvements in programming speed.



Programming of a flash device through Boundary Scan

In-Application Programming (IAP)

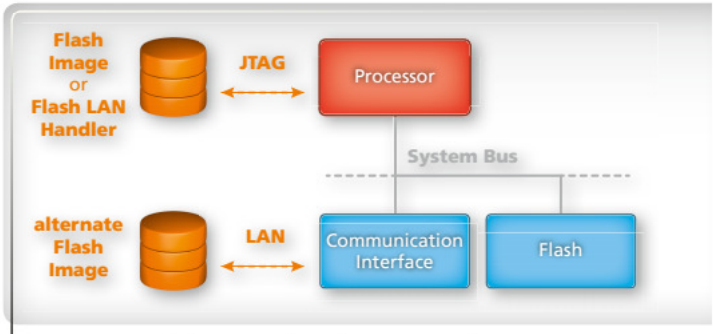
In the case of the **IAP** method, a flash programming routine is added to the native firmware. This routine serves to reprogram flash devices connected to the processor while the system is running, by means of a command. The required flash image is provided by an external interface (e.g. a LAN).



Flash device programming through In-Application Programming (**IAP**)

Core Assisted Programming (CAP)

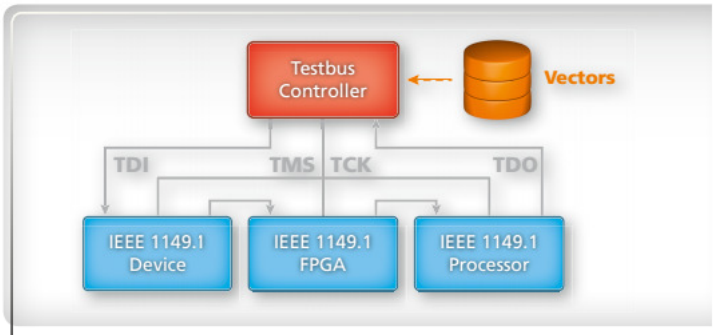
The premise of the **Core-Assisted Programming** (CAP) strategy is similar to processor emulation testing. The processor is controlled through its native debug interface in such a way that allows flash or FPGA (design permitting) connected to the system bus to be erased, programmed, and verified. In the case of flash it does not matter whether it is integrated in the micro controller unit (on-chip flash) or connected as external, discrete flash device. Furthermore, it is possible to load only the flash handler/programming engine via JTAG into the processor and to download the flash data image through a high-speed communication interface on the processor. CAP technology provides a much higher In-System Programming speed than Boundary Scan based device programming.



Programming flash memory through Core-assisted Programming (**CAP**)

System JTAG (SJTAG)

While remote control via an external controller is possible, **System JTAG** typically employs a central test control unit integrated directly into the system design. Test vectors are usually stored locally on the system and a separate IC is commonly used as the test bus controller. There is currently a SJTAG initiative in progress to standardise this process.



Integration of test bus controllers in **SJTAG**

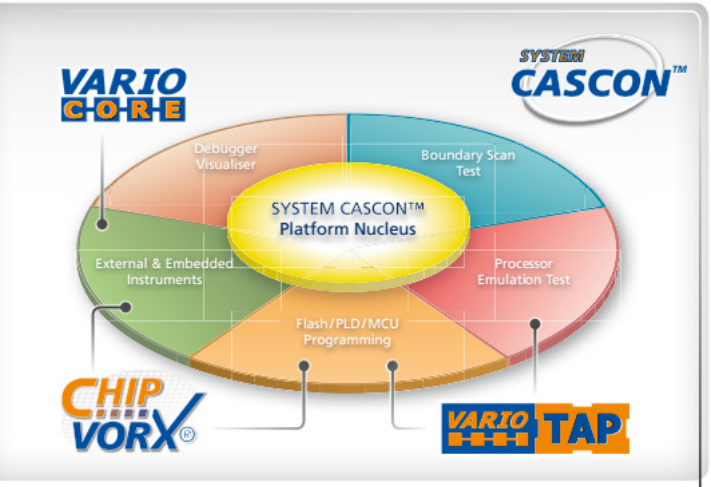
Software IP-based Technology from GOEPEL electronic

Software Reconfigurable Instruments

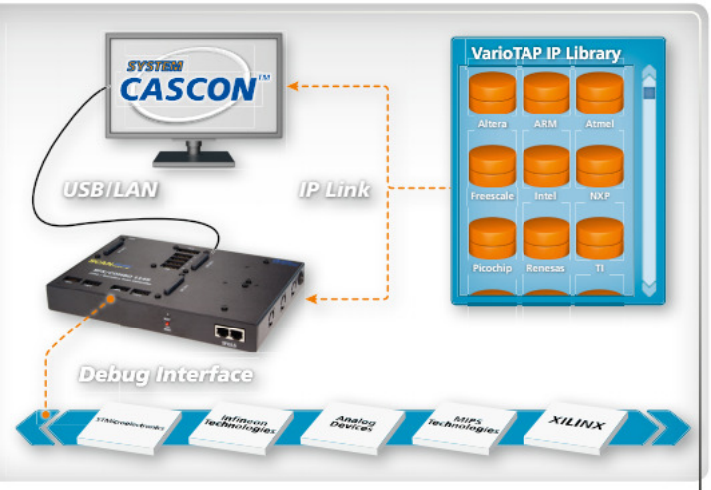
There is no doubt that the **growing number of ESA technologies** are making possible a continuous improvement in the control problems prevalent while testing, programming and validating state-of-the-art electronics at chip, board, and system level. In contrast, **vendors** of proper testing equipment **are facing a severe challenge**. GOEPEL electronic detected this problem early on and pursued the **approach** known as „**Software Reconfigurable Instruments**". This aims to dynamically adapt hardware and software tools to the actual target mission by means of appropriate IPs. The system is essentially based on the following technologies:

- SYSTEM CASCON™ – software platform
- SCANFLEX® – hardware platform
- VarioTAP® – processor IP
- ChipVORX® – instrument IP
- VarioCore® – I/O module IP

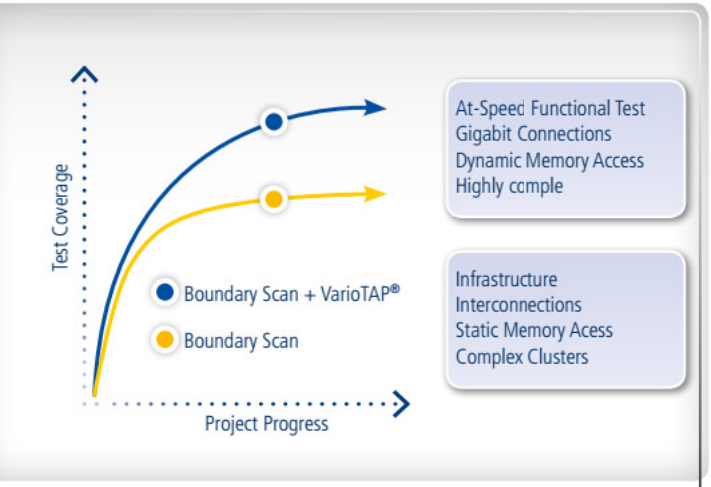
By integrating the IP-based technologies into SYSTEM CASCON, the original boundary scan **tool suite** was developed into an open software/ hardware-related platform **that supports all ESA strategies**.



Integration of IP technologies into **SYSTEM CASCON™**



Example of the functional principle of **VarioTAP®**



Improvement of fault coverage by **VarioTAP®**

Technology	SYSTEM CASCON	VarioTAP	ChipVORX
Boundary Scan Test	✓	-	-
Processor Emulation Test	-	✓	-
Chip-embedded Instruments	✓*	-	✓
Embedded Diagnostics Test	-	✓	-
In-System Programming	✓	-	✓
Core-Assisted Programming	-	✓	-
FPGA-Assisted Programming	-	-	✓

*limited to the simplest instruments

Moreover, the overall solution also enables deep interaction with many conventional access technologies such as In-Circuit Testing, Flying Probe Testing and Functional Testing. Further information in this regard is available at **goepel.com/en/products** and **goepel.com/en/integration**. The specific IP-based technologies are described in more detail below.

VarioTAP® Technology

VarioTAP is a revolutionary technology for the **fusion of Boundary Scan and processor emulation**. It uses VarioTAP models to adapt platform modules to the target processor. The models are modularly defined as intelligent software IP and basically offer a multi-level functional structure.

- core-assisted flash programming / PLD programming
- bus emulation test / system emulation test
- Embedded Diagnostics Test (EDT)

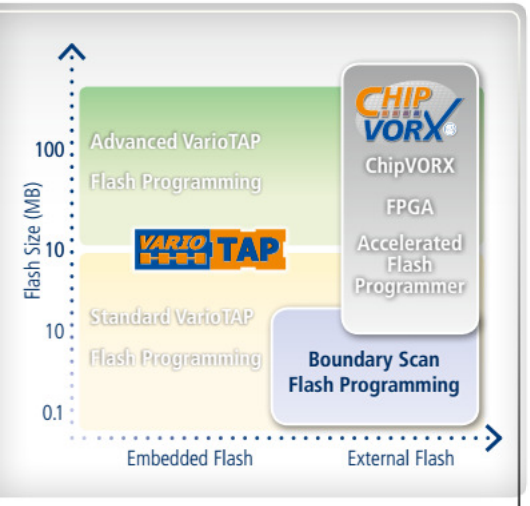
In principle it is possible – **in combination with SCANFLEX** hardware, which is also adapted dynamically through software to the corresponding debugging interface (JTAG, BDM, SBW, SWD, COP, etc.) – to support all contemporary processors and micro controllers. The same applies to multi-processor and multi-core designs. This makes VarioTAP the leading Processor Emulation Technology available on the market.

Further information on **Embedded System Access** as well as on technologies and products is available at

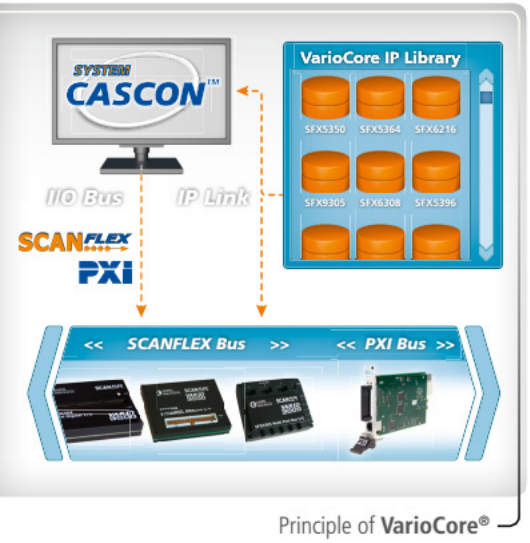
goepel.com/**en/variotap**

IP Technology for Chip-embedded Instruments and I/O Modules

ChipVORX® controllers for soft and hard macros



ChipVORX® drives flash-ISP performance



Principle of **VarioCore®**

ChipVORX® Technology

Thanks to innovative ChipVORX technology, it was possible to **combine Boundary Scan and Chip-embedded Instruments** for the first time. ChipVORX models are used to adapt software tools to the target instruments. As a result, the technology is completely open for any type of instrument.

- FPGA-loaded instruments (soft macros)
- IP vendor proprietary instruments (hard macros)
- standardised instruments access (IJTAG macros)
- custom-designed instruments (ASIC hard macro)

IC-centered ChipVORX models are functional software IPs with a modular architecture. This openness serves to simultaneously support several embedded instruments. The same applies if the instruments are embedded in different chips. FPGA-based instruments are particularly significant, because they enable extremely flexible applications. In this case, too, ChipVORX offers an excellent solution, because it supports ESA technologies such as **FPGA-Assisted Test** (FAT) and **FPGA-Assisted Programming** (FAP); at the same time, it is able to handle soft macros and the required loading into the target FPGA. This means that ChipVORX models for FPGA are not only able to access and control instruments, they can also contain such instruments. This type of ChipVORX model focuses on applications such as:

- high-speed flash In-System Programming
- high-speed access test of DDR-SDRAM
- universal frequency and clock measurements
- bit error rate test (BERT)

VarioCore® Technology

VarioCore is a revolutionary technology for the **reconfiguration of I/O modules**. These modules include:

- SCANFLEX I/O modules (digital/mixed signal)
- PXI I/O modules (digital)

VarioCore IPs, which dynamically adjust the functional scope of a module to the appropriate test task, serve as their basis. In doing so, the VarioCore IPs can be activated in sequence and can be immediately accessed and controlled, i.e. without having to reinitialise the platform. The available functions include:

- counter/frequency measurement IP
- vector generator/recorder IP
- digitiser/bus emulator IP
- customer-specific IP

Get the total Coverage!

The interaction between **VarioCore®, ChipVORX® and VarioTAP® on a single platform** provides superior flexibility in any dimension – Get the total Coverage!

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Get the total Coverage!
ISO 9001 certified

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